SHARP®

## DVD Video Player

# SERVICE MANUAL

## MODELS

**DV-SV92S(Y,RU,B,U)**

In the interests of user-safety (Required by safety regulations in some countries) the set should be restored to its original condition and only parts identical to those specified be used.

## CONTENTS




**SHARP CORPORATION**

# 1. GENERAL DESCRIPTION

## 1.1 ES6809 Vibratto-II CL DVD Processor

## DESCRIPTION

The ES6809 Vibratto™II CL processor is a single chip DVD system on chip with DivX®, MPEG-4, and DVD video playback. The ES6809 integrates all front-end DVD servo control functions including read channel, ECC, servo DSP, MCU for high performance disc read and a high quality TV encoder for a brilliant 480p/576p progressive scan video output with Macrovision™ copy protection. The ES6809 is an ideal solution for stand-alone DVD players, DVD receivers, DVD/VCR combos and DVD A/V minicomponent systems.
The ES6809 is built on the ESS proprietary dual CPU Programmable Multimedia Processor (PMP) core consisting of 32-bit RISC and 64-bit DSP processors that deliver the best DVD feature set. This PMP core, common through out all generations of Vibratto DVD products, allows for easy migration from previous ESS based designs. The processing units enable simultaneous parallel execution of system commands and data processing to perform specialized encoding and decoding tasks. The vector engine performs audio and video processing to support MPEG, Dolby®, DTS™, JPEG and DivX standards.
The front-end servo control of the ES6809 supports all popular optical pick-up units (OPU). Its high performance error handling allows for playback of scratched and fingerprinted media. The ES6809 has a unified memory architecture for both the front-end servo control and backend decoder to achieve the lowest possible system memory cost.
The ES6809 has unmatched audio features including an integrated high quality stereo audio digital to analog converter (DAC) and an analog to digital converter (ADC).
Additionally, the ES6809 supports DVD-Audio, CD-DA, HDCD, MP3, WMA, AAC, Dolby ProLogic™ II digital audio formats and Karaoke.
The ES6809 CL DVD processor with DTS support is offered with the ES6809D, which has the same pinout as the standard ES6809. The ES6809 and ES6809D processors are in 208-pin Plastic Quad Flat Pack (PQFP) device package.

## FEATURES

- DVD SoC incorporating all front-end DVD servo control and back-end DVD decode.
- DivX Home Theater quality video at full screen (D1).
- MPEG-4 Advanced Simple Profile video.
- DVD-Audio multi-channel playback including MLP and 24-bit LPCM decode, CPPM decryption and watermark detection
- DVD-Video, DVD-R/RW, DVD+R/RW, SVCD, VCD, CDROM, CD-R/RW, CD-DA.
- High-performance focusing, sledding, tracking and CLV/CAV spindle servo control.
- Integrated stereo audio DAC and audio ADC.
- Integrated NTSC/PAL encoder with pixel-adaptive deinterlacer
- Five 54 MHz VDACs for simultaneous composite, Svideo and YUV video outputs.
- Macrovision NTSC/PAL interlaced and progressive scan (480p/576p) video output
- Direct interface of 16-bit DRAM with up to 128-Mb capacity
- Direct interface for up to 4 banks of 8-bit EPROM or Flash memory with up to 4 MB per bank
- CCIR656/601 YUV 4:2:2 input/output
- OSD controller supports 256 colors in 8 degrees of transparency
- Sub-picture Unit (SPU) decoder supports karaoke lyric, subtitles and EIA-608 compliant Line 21 captioning.
- Dolby Digital, Dolby ProLogic, and Dolby ProLogic II
- DTS Digital Out

• SRS TruSurround®
• MPEG Multichannel, AAC, MP3.
• SPDIF digital audio input and output
• JPEG digital photo support (Kodak Picture CD™ and Fujifilm FujiColor CD™)

## 1.2 MEMORY

### 1.2.1 System SRAM Interface

The system SRAM interface controls access to optional external SRAM, which can be used for RISC code, stack, and data. The SRAM bus supports four independent address spaces, each having programmable bus width and wait states. The interface can support not only SRAM, ROM/EPROM and memory-mapped I/O ports for standalone applications are also supported.

### 1.2.2 DRAM Memory Interface

The Vibratto-II CL provides a glueless 16-bit interface to DRAM memory devices used as video memory for a DVD player. The maximum amount of memory supported is 16 MB of Synchronous DRAM (SDRAM). The memory interface is configurable in depth to support 128-Mb addressing. The memory interface controls access to both external SDRAM or EDO memories, which can be the sole unified external read/write memory acting as program and data memory as well as various decoding and display buffers.

## 1.3 FRONT PANEL

The front panel is based around an VFD and a common NEC (or compatible) front panel controller chip, (uPD16311). The chipset ES6809 controls the uPD16311 using several control signals, (clock, data, chip select). The infrared remote control signal is passed directly to the ES6809 for decoding.

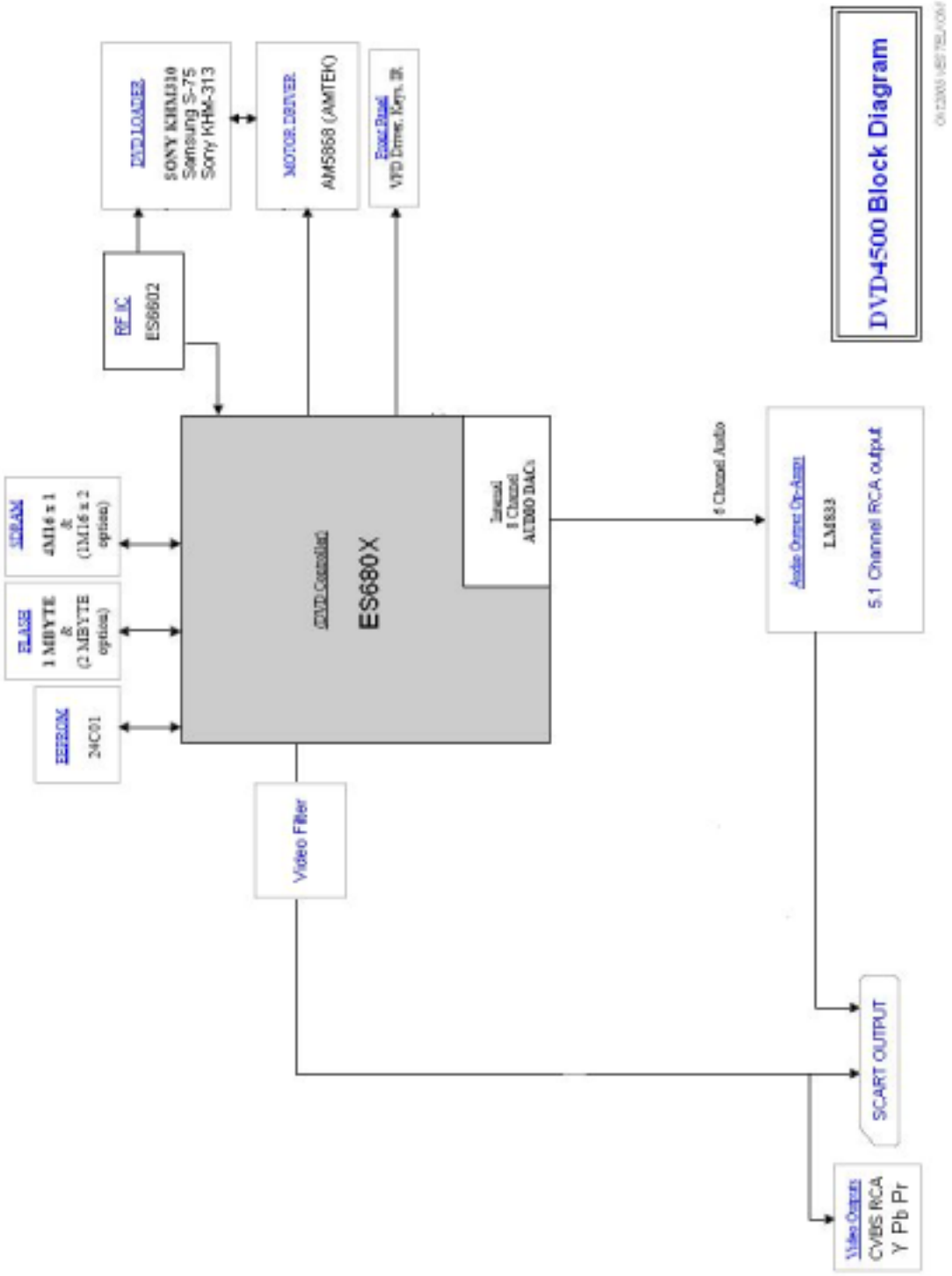
## 1.4 Back PANEL

A typical rear panel is included in the reference design. This rear panel supports:

- Two channel audio outputs
- Optical and coax S/PDIF outputs.
- Composite, SCART outputs

The six-video signals used to provide CVBS and RGB are generated by the ES6809's internal video DAC. The video signals are buffered by external circuitry.

## 2. SYSTEM BLOCK DIAGRAM and ES6809 PIN DESCRIPTION

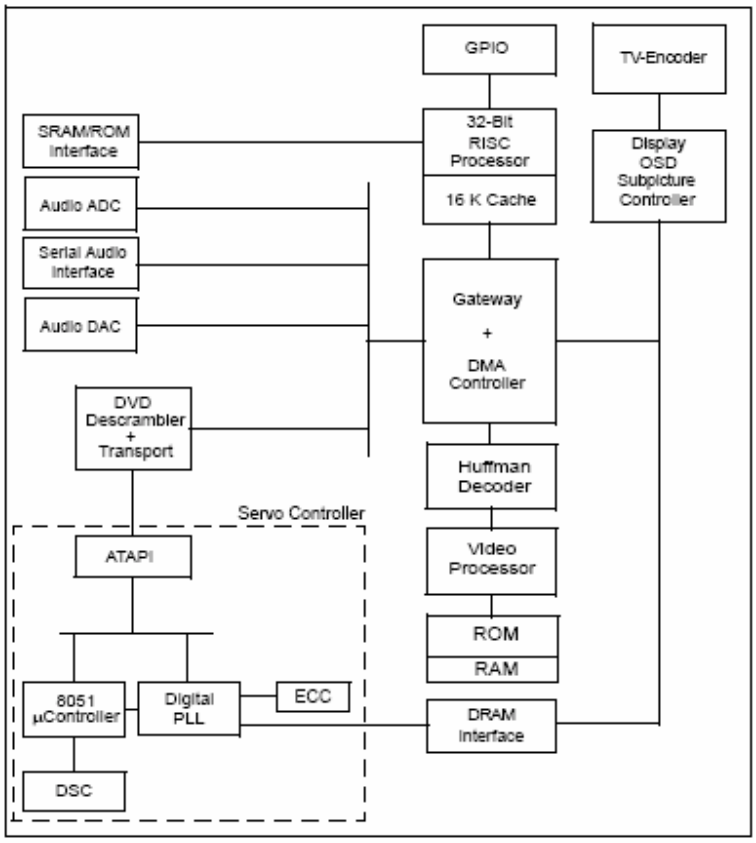


**ES6809 PIN DESCRIPTION**

| Names | Pin Numbers | I/O | Definitions |
|---|---|---|---|
| VD33 | 1, 11, 20, 36, 45, 53, 63, 80, 97, 122, 130, 156, 182, 197 | P | I/O power supply. |
| AUX0 | 2 | I/O | Host control 0. |
| AUX3 | 3 | I/O | Auxiliary port 3. |
| RESET# | 4 | I | Reset (active-low). |
| AUX1 | 5 | I/O | Host control 1. |
| DMA11:0 | 6:9, 12:18, 21 | O | DRAM address bus. |
| VSS | 10, 19, 27, 35, 44, 52, 62, 72, 79, 87, 96, 123, 133, 138, 183, 196, 201, 208 | G | Ground. |
| DRAS2-0# | 22, 23, 26 | O | DRAM row address strobes (active-low). |
| DCS1-0# | 24, 25 | O | DRAM chip selects (active-low). |
| VDD | 28, 73, 88, 134, 202 | P | Core power supply. |
| DCAS# | 29 | O | DRAM column address strobe (active-low). |
| DOE# | 30 | O | DRAM output enable (active-low). |
| DWE# | 31 | O | DRAM write enable (active-low). |
| DSCK | 32 | O | Output clock to DRAM. |
| DQM | 33 | O | Data input/output mask. |
| DB15-0 | 34, 37:43, 46:51, 54, 55 | I/O | DRAM data bus. |
| LA21-0 | 56:61, 64:67, 69:71, 74:78, 81:83, 101 | O | SRAM address bus. |
| LWRLL# | 68 | O | SRAM bus write enable (active-low). |
| LCS3-0# | 84:86, 89 | O | SRAM bus chip select (active-low). |
| LD7-0 | 90:95, 98, 99 | I/O | SRAM data bus. |
| LOE# | 100 | O | RISC port output enable (active-low). |
| SPDIF_OUT | 102 | O | S/PDIF output. |
| SPDIF_IN | 103 | I | S/PDIF input. |
| VD33PLL | 104 | P | Power for PLL blocks. |
| VS33PLL | 105 | G | Ground for PLL blocks. |
| VREF | 106 | I | Internal voltage reference to video DAC. |
| COMP | 107 | I | Compensation input. |
| RSET | 108 | I | DAC current adjustment resistor input. |
| FDAC | 109 | O | Video DAC output. |
| VDAC | 110 | O | Video DAC output. |
| VD33_DA | 111 | P | Power for I/O power supply for VDAC. |
| VS33_DA | 112 | G | Ground for I/O power supply for VDAC. |
| YDAC | 113 | O | Video DAC output. |
| CDAC | 114 | O | Video DAC output. |
| UDAC | 115 | O | Video DAC output. |
| ADC_BIAS | 116 | O | Audio ADC bias voltage out. |
| MIC | 117 | I | Audio ADC MIC 1. |
| ADC_CAP | 118 | O | Audio ADC output capacitance. |
| TWS | 119 | O | Audio transmit frame sync output. |
| TSD0 | 120 | O | Audio transmit serial data port 0. |
| TSD1 | 121 | O | Audio transmit serial data port 1. |

| | | | |
|---|---|---|---|
| TSD2 | 124 | O | Audio transmit serial data port 2. |
| TSD3 | 125 | O | Audio transmit serial data port 3. |
| TBCK | 126 | O | Audio transmit bit clock. |
| TXD0 | 127 | I/O | Serial port 0 transmit. |
| RXD0 | 128 | I/O | Serial port 0 receive. |
| MCLK | 129 | I/O | Audio master clock for audio DAC. |
| TXD1 | 131 | I/O | Serial port 1 transmit. |
| RXD1 | 132 | I/O | Serial port 1 receive. |
| AUX3[5] | 135 | I/O | Aux3 data I/O 5. |
| AUX3[0] | 136 | I/O | Aux3 data I/O 0. |
| TX | 137 | I | Zero crossing of TE. |
| RX | 139 | I | Zero crossing of RF envelope. |
| LDCO | 140 | O | CD/DVD laser diode select. |
| LG | 141 | O | DVD-RAM land/groove flag for next track. |
| IP2 | 142 | I | DVD-RAM header position index 2. |
| SDEN | 143 | O | RF chip serial data enable. |
| SDATA | 144 | I/O | Data signal to/from RF chip. |
| SCLK | 145 | O | Serial clock source to RF chip. |
| DFCT | 146 | I | Defect flag input signal. |
| MIRR | 147 | I | Mirror detect input. |
| LDON | 148 | O | Laser diode on/off control. |
| BSUM | 149 | I | Photodiode subbeam addition input signal. |
| FE | 150 | I | Focus input error signal. |
| CE | 151 | I | Center error input signal. |
| TE | 152 | I | Tracking error input. |
| RFENV | 153 | I | RF ripple envelope input signal. |
| VREFOUT | 154 | I | Reference voltage for servo analog output signals. |
| VREFIN | 155 | I | Reference voltage for servo analog input signals. |
| DMO | 159 | O | Spindle drive. |
| FOO | 160 | O | Focus drive. |
| SLO | 161 | O | Sled drive. |
| RPBC | 162 | O | RF envelope balance control. |
| TRO | 163 | O | Track drive. |
| NC | 164 | O | No connect. |
| TEBC | 165 | O | Tracking error balance control. |
| REFD | 166 | I | Flash reference decouple. |
| IN_M | 167 | I | Analog RF signal (minus). |
| IN | 168 | I | Analog RF signal (plus). |
| AVDD3 | 169 | P | 3.3V analog power for flash. |
| AVSS | 170 | G | Analog ground for flash. |
| DVCC | 171 | P | 1.8V power for flash. |
| IP1 | 172 | I | DVD-RAM header position index 1. |
| IDSEL | 173 | I/O | DVD-RAM detected signal of ID area. |
| AMPSTBY | 174 | O | Power amplifier standby. |
| FGIN | 175 | I | Spindle hall sensor input. |
| CLOSESW | 176 | I | Tray closed detector. |
| HOMESW | 177 | I | Sled home switch position detector. |
| CLOSE | 178 | O | Drive to close tray. |

| | | | |
|---|---|---|---|
| OPENSW | 179 | I | Tray open detector. |
| OPEN | 180 | O | Drive to open tray. |
| MDET | 181 | I | Spindle drive motor rotation direction detect. |
| AUX7 | 184 | I/O | Auxiliary port 7. |
| AUX3[7] | 185 | I/O | Aux3 data I/O 7. |
| EAUX1 | 186 | I/O | Extended auxiliary port 1. |
| AUX3[6] | 187 | I/O | Aux3 data I/O 6. |
| EAUX0 | 188 | I/O | Extended auxiliary port 0. |
| EAUX3 | 189 | I/O | Extended auxiliary port 3. |
| EAUX2 | 190 | I/O | Extended auxiliary port 2. |
| VSYNC# | 191 | I/O | Vertical sync (active-low); (5V tolerant input). |
| HSYNC# | 192 | I/O | Horizontal sync (active-low); (5V tolerant input). |
| XI | 193 | I | Crystal clock in. |
| XO | 194 | O | Crystal clock out. |
| AUX3[4] | 198 | I/O | Aux3 data I/O 4. |
| AUX3[1] | 199 | I/O | Aux3 data I/O 1. |
| AUX3[3] | 200 | I/O | Aux3 data I/O 3. |
| AUX3[2] | 203 | I/O | Aux3 data I/O 2. |
| AUX6-4, 2 | 204-207 | I/O | Auxiliary ports 2, 4, 5 and 6; (5V tolerant input). |



## 3. Audio Interface

The audio interface is a bidirectional serial port that connects to an external audio ADC/DAC for the transfer of PCM (pulse coded modulation) audio data in $I_2S$ format. It supports 16-, 24-, and 32-bit audio frames. No external master clock is required.
The ES6809 offers three audio interface modes:
1. Stereo mode using TSD0 pin 120.
2. Dolby Digital (AC-3) 5.1 channel mode using TSD[3:0] pins 120, 121, 124, and 125.
3. Dolby Digital (AC-3) 5.1 channel mode using S/PDIF pins 102 and 103.

## 4. Audio Performance

Table 36 lists the audio performance characteristics of the digital audio processor of the ES6809 under normal operating conditions (AVCC = 3.3V ±10%, DVCC =2.5±10%, TAMB 0 to 70°C).

| **Parameter** | **Typical Unit** |
|---|---|
| ADC Resolution | 16 Bit |
| ADC Data Sample Rate | 192 KHz |
| ADC Dynamic Range | 80 dB |
| ADC THD | 1 % |
| DAC Resolution | 24 Bit |
| DAC Sample Rate | 192 KHz |
| DAC THD+Noise | 75 dB |
| DAC Dynamic Range | 88 dB |
| DAC Bandwidth | 20 KHz |

# 5 VIDEO INTERFACE

**Video Display Output**
The video output section controls the transfer of video frames stored in memory to the internal TV encoder of the Vibratto. The output section consists of a programmable CRT controller capable of operating either in Master or Slave mode.

The video output section features internal line buffers which allow the outgoing luminance and chrominance data to match the internal clock rates with external pixel clock rates, easily facilitating YUV4: 2:2 to YUV4: 2:0 component and sample conversion. A polyphase filter achieves arbitrary horizontal decimation and interpolation.

**Video Bus**
The video bus has 8 YUV data pins that transfer luminance and chrominance (YUV) pixels in CCIR601 pixel format (4:2:2). In this format, there are half as many chrominance (U or V) pixels per line as luminance (Y) pixels; there are as many chrominance lines as luminance.

**Video Post-Processing**
The Vibratto video post-processing circuitry provides support for the color conversion, scaling, and filtering functions through a combination of special hardware and software. Horizontal up-sampling and filtering is done with a programmable, 7-tap polyphase filter bank for accurate non-integer interpolations. Vertical scaling is achieved by repeating and dropping lines in accordance with the applicable scaling ratio.

**Video Timing**
The video bus can be clocked either by double pixel clock and clock qualifier or by a single pixel clock. The double clock typically is used for TV displays, the single for computer displays.

# 6 SDRAM MEMORY

The ES6809 provides a glueless 16-bit interface to DRAM memory devices used as video memory for a DVD player. The maximum amount of memory supported is 16 MB of Synchronous DRAM (DRAM). The memory interface is configurable in depth to support 128-Mb addressing.

Typical SDRAM Configurations:

| Mem. Size (MB) | Bit Order | | | | Memory Configuration (Mb per pc) |
|---|---|---|---|---|---|
| | SD64M | SD8BIT | SDCFG1 | SDCFG0 | |
| 2 | 0 | 0 | 0 | 1 | 1 pc: 512Kx16x2 (16 Mb) |
| 4 | 0 | 0 | 0 | 0 | 2 pcs: 512Kx16x2 (16 Mb) |
| 4 | 0 | 1 | 0 | 1 | 2 pcs: 1Mx8x2 (16 Mb) |
| 8 | 0 | 1 | 0 | 0 | 4 pcs: 1Mx8x2 (16 Mb) |
| 8 | 1 | 0 | X | X | 1 pc: 1Mx16x4 (64 Mb) |
| 16 | 1 | 0 | X | X | 2 pc: 1Mx16x4 (64 Mb) |
| 16 | 1 | 1 | X | X | 2 pc: 2Mx8x4 (64 Mb) |
| 16 | 1 | 1 | X | X | 1 pc: 2Mx16x4 (128 Mb) |

The memory interface controls access to both external SDRAM or EDO memories, which can be the sole unified external read/write memory acting as program and data memory as well as various decoding and display buffers. At high clock speeds, the Vibratto memory bus interface has sufficient bandwidth to support the decoding and displaying of CCIR601 resolution images at full frame rate.

# 7 FLASH MEMORY

The decoder board supports AMD class Flash memories. Currently 4 configurations are supported:

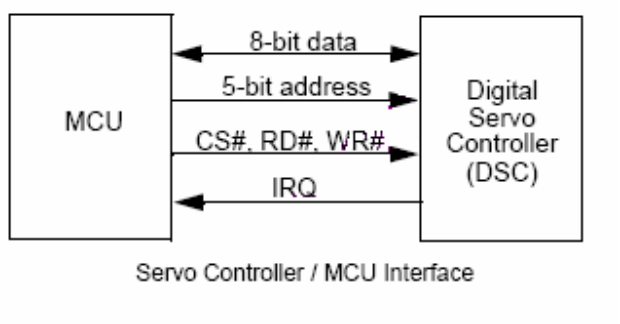
FLASH_512K_8b
FLASH_1024K_8b
FLASH_512Kx2_8b
FLASH_512Kx2_16b

The Vibratto permits both 8- and 16-bit common memory I/O accesses with a removable storage card via the host interface.

# 8 SERIAL EEPROM MEMORY

An I2C serial EEPROM is used to store user configuration (i.e. language preferences, speaker setup, etc.) and software configuration.. Industry standard EEPROM range in size from 1kbit to 256kbit and share the same IC footprint and pinout. The default device is 2kbit, 256kx 8, SOIC8 SGS Thomson ST24C02M1 or equivalent.

## 9 Digital Servo Controller



Servo Controller / MCU Interface

The digital servo includes an internal DSP, on-chip RAM and ROM, control logic, a loader interface, a serial interface, and an on-chip ADC-DAC, and interfaces with the MCU.
The MCU handles the high-level functions of optical disk and front-end system control. The interface between the servo controller and the MCU is illustrated in the Figure.

# 10 Front Panel

### VFD Controller

The VFD controller is a NEC uPD16311. This controller is not a processor, but does include a simple state machine which scans the VFD and reads the front panel button matrix. The 16311 also includes RAM so it can store the current state of all the VFD icons and segments. Therefore, the 16311 need only be accessed when the VFD status changes and when the button status is read. The ES6809 can control this chip directly using PIO pins or can allow the front panel PIC to control the VFD.

## 11 Reset Circuitry & Voltage Regulators

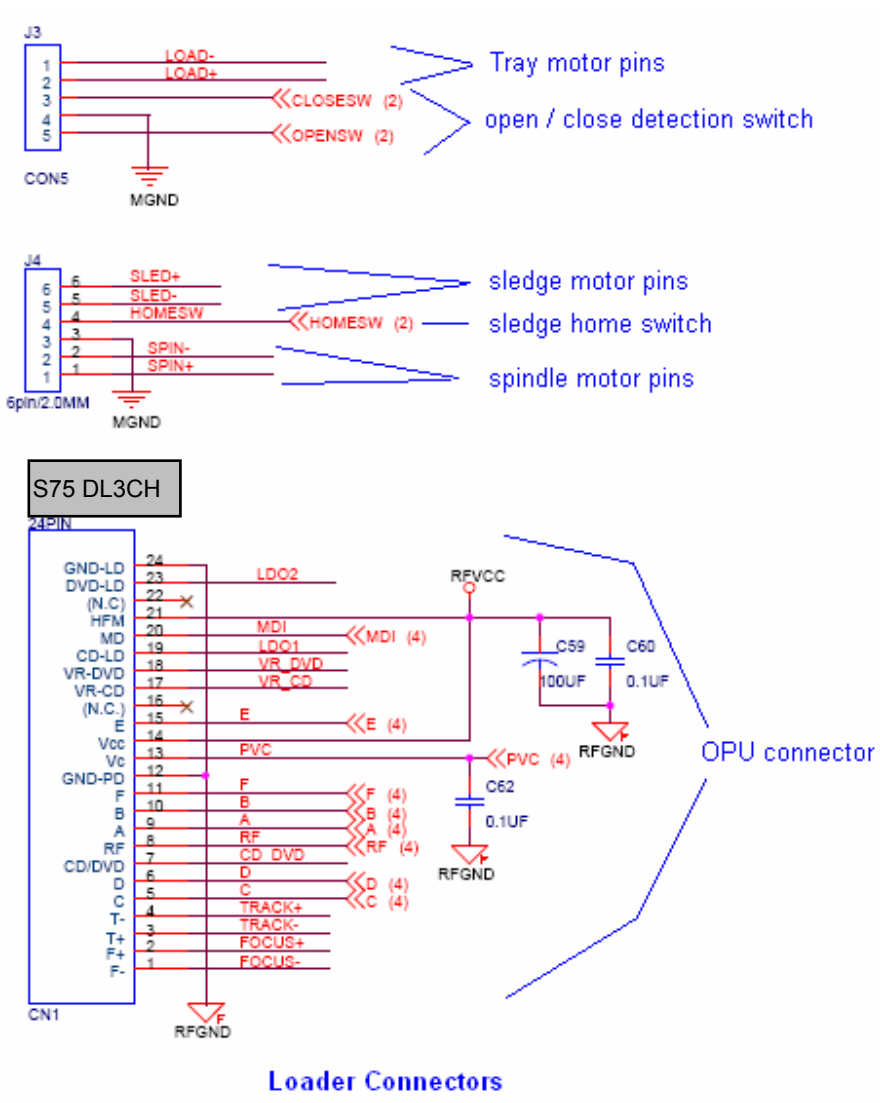
Two different chips are supported to provide the power-on-reset AAT3521 or AAT3520.

Voltage regulators:

U6: LM1117(1.8V) For 2V PLL power supply
U19: 7805 For 5V power supply

# 12 CONNECTORS

## 12.1 LOADER CONNECTORS:




**Loader Connectors**

## 12.2 SCART CONNECTOR

| Pin | Function | Signal Level | Impedance |
|---|---|---|---|
| 1 | audio right out (or audio mono out) | 0.5v rms | < 1K ohm |
| 2 | audio right in (or audio mono in) | 0.5v rms | > 10 K ohm |
| 3 | audio left out (or audio mono out) | 0.5v rms | < 1K ohm |
| 4 | audio ground | | |
| 5 | blue ground | | |
| 6 | audio left in (or audio mono in) | 0.5v rms | > 10K ohm |
| 7 | blue | 0.7v | 75 ohms |
| 8 | function select | 9.5–12V = AV mode<br>5–8V = widescreen mode<br>0–2V = TV mode | > 10K ohm |
| 9 | green ground | | |
| 10 | data 2 | | |
| 11 | green | 0.7v | 75 ohms |
| 12 | data 1 | | |
| 13 | red ground | | |
| 14 | data ground | | |
| 15 | red | 0.7v | 75 ohms |
| 16 | RGB control | 1–3v = RGB,<br>0–0.4v = composite | 75 ohms |
| 17 | video ground | | |
| 18 | RGB control ground | | |
| 19 | composite video out | 1v | 75 ohms |
| 20 | composite video in | 1v | 75 ohms |
| 21 | safety ground | | |

**SCART Connector Signals (Composite and RGB Video).**

Some cheaper SCART cables use unshielded wires, which is just about acceptable for short cable lengths. For longer lengths, shielded co-ax cable become essential.

## Scart Signals:

**Audio signals**
0.5V RMS, <1K output impedance, >10K input impedance.

**Red, Green, Blue**
0.7Vpp ±2dB, 75R input and output impedance. Note that the Red connection (pin 20) can alternatively carry the S-VHS Chrominance signal, which is 0.3V.

**Composite Video / CSync**
1Vpp including sync, ±2dB, 75R input and output impedance.Bandwidth = 25Hz to 4.8MHz for normal TV Video de-emphasis to CCIR 405.1 (625-line TV)

**Fast Blanking**
75R input and output impedance. This control voltage allows devices to over-ride the composite video input with RGB inputs, for example when inserting closed caption text. It is called fast because this can be done at the same speeds as other video signals, which is why it requires the same 75R impedances.

**0 to 0.4V**: TV is driven by the composite video input signal (pin 19). Left unconnected, it is pulled to 0V by its 75R termination.

**1V to 3V**: the TV is driven by the signals Red, Green, Blue and composite sync. The latter is sent to the TV on pin 19. This signal is useful when using a TV to display the RGB output of devices such as home computers with TV-compatible frame rates. Tying the signal to 5V via 100R forms a potential divider with the 75R termination, holding the signal at around 2V. Alternatively, if a TTL level (0 to 5V) negative sync pulse is available, this will be high during the display periods, so this can drive the blanking signal via a suitable resistor.

**Control Voltage**

**0 to 2V** = TV, Normal.
**5 to 8V** = TV wide screen
**9.5 to 12V** = AV mode

# 13. CIRCUIT DESCRIPTION

## 13.1 POWER SUPPLY:

- Socket PL2 is the 220VAC input.
- 2.5A fuse F1 is used to protect the device against short circuit and unexpected overloads.
- Voltage is rectified by using D1-D2-D3-D4 diodes. Using capacitor C33,C34 (47∝f) a DC voltage is produced. (310- 320VDC).
- The current in the primary side of the transformer TR2 comes to the SMPS IC (TNY267P). It has a built-in oscillator, overcurrent and overvoltage protection circuitry. It starts with the current from the primary side of the transformer and follows the current from the feedback winding.
- Feedback current is deteceted by optocoupler IC2. Depending on the control current coming from the secondary side, SMPS IC keeps the output voltage constant by controlling the duty cycle of the PWM at the primary side of the transformer.
- Voltages on the secondary side are as follows: +12 Volts at D20, +5 Volts at D12, +3.3V at D13, -22V D19, Using the output of the D25, a photo diode inside of the IC2 generates feedback signal bu using optocoupler's photo transistor. This photo transistor adjusts the control voltage at the IC3. The voltage at this pin effects the pwm output frequency on the IC3 pin5 (Drain pin). And finally output voltages reach their correct values by this way.

- –22 Volts is used to feed the VFD (Vacuum Fluorescent Display) driver IC on the front panel.

## 13.2 FRONT PANEL:

- All the functions on the front panel are controlled by ES6809 on the mainboard. Key scanning and IR checking operations on the standby mode are controlled by VFD driver IC (uPD16311).
- ES6809 IC sends the commands to uPD16311 via socket J2 (pins 2,3 and 4).
- There are 16 keys scanning function, 2 LED outputs, 1 Stand-by output and VFD drivers on the uPD16311 IC.
- Front panel LED is bright red in stand-by mode and green when the device is turned on.
- IR remote control receiver module (TSOP1836) sends the commands from the remote control directly to the ES6809.

# CD Update Procedure of DV-SV92

1. Download the update file from the convenient link according to your default language choice.

2. While there is no CD in the DVD (No Disc Mode) , press “Menu 1 3 5 7” buttons on the remote control in order to reach the Service Menu of DVD Player:


   2.1. Note the software version described as “b.xx “ to be able to compare the sw. Version after update process.

3. Copy the update file to the desktop and rename it according to the update file name in the hidden menu of the device.
   For example If M2101RP_ is written then rename it like M2101RP_.rom
   If S6111___ is written then rename it like S6111___.rom

   (If you receive the update file already renamed (with addition of .rom) from the customer technical support department by giving the SAP code of the product then burn the already renamed file with nero program as it is shown below.)


4. Burn the renamed files by Nero program with below set up.

5. After burning process is completed, place the update CD into the DVD tray and press play button.

6. Wait to see the update process steps as shown below. When the sw. Update is completed unit will switch itself to standby mode.


7. Finally, press the eject button and take out the update CD while DVD Player remains at stand by Mode.

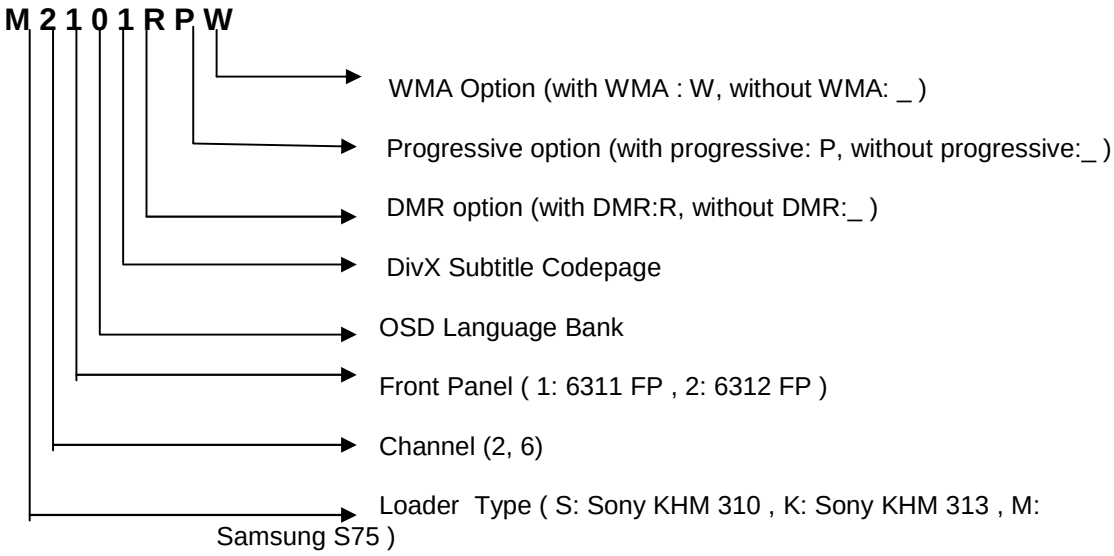
8. Updating process has been completed. To check whether it is updated correctly or not, repeat the first step for comparing software version

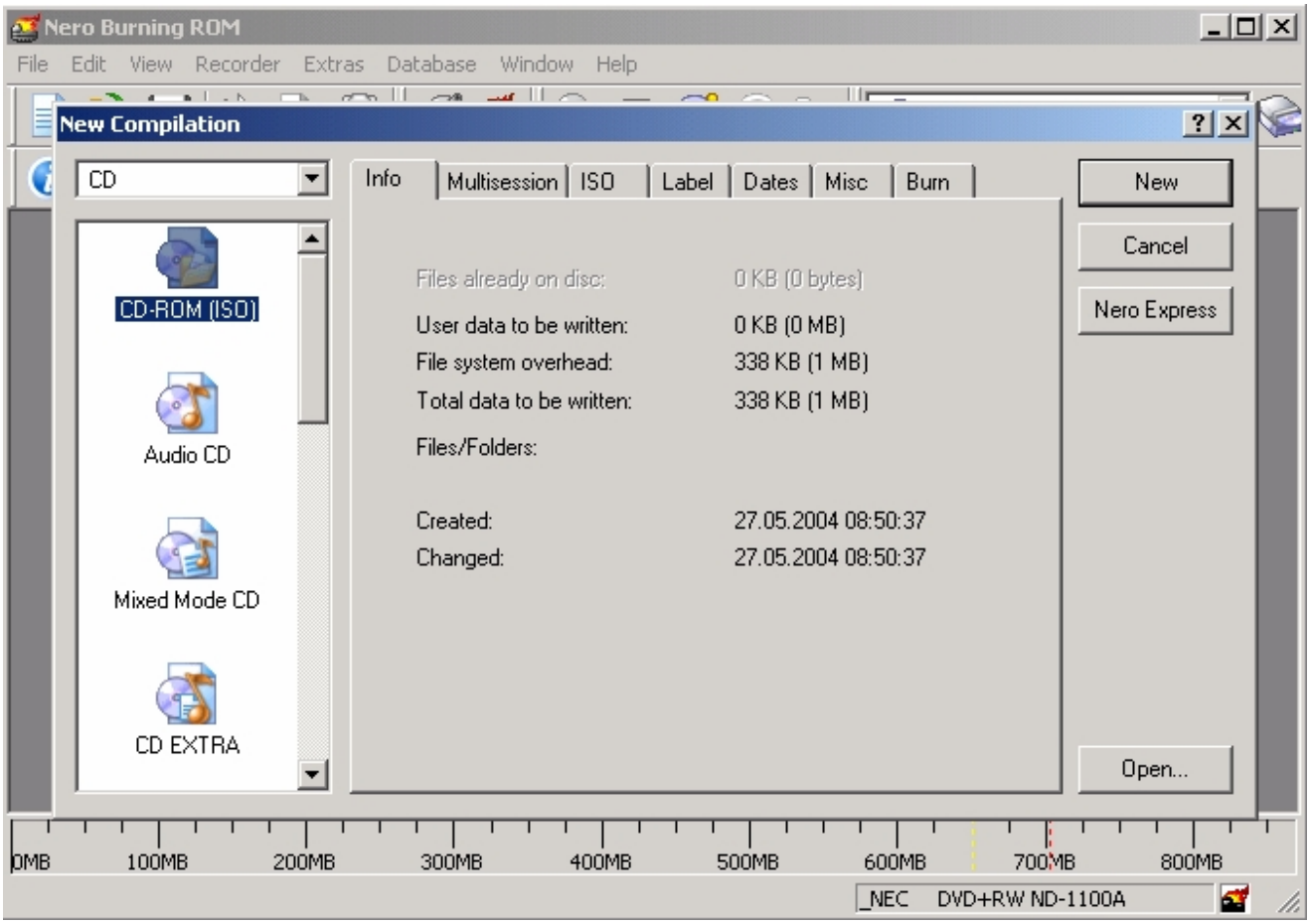
9. If the previous and letter names are different, CD is update has completed successfully. If the name remains same than go through the steps from the beginning.

**IMPORTANT NOTE: If the AC source breaks down while the updating the unit (main board) will be totally out of order. This kind of units/boards is out of Warranty.**

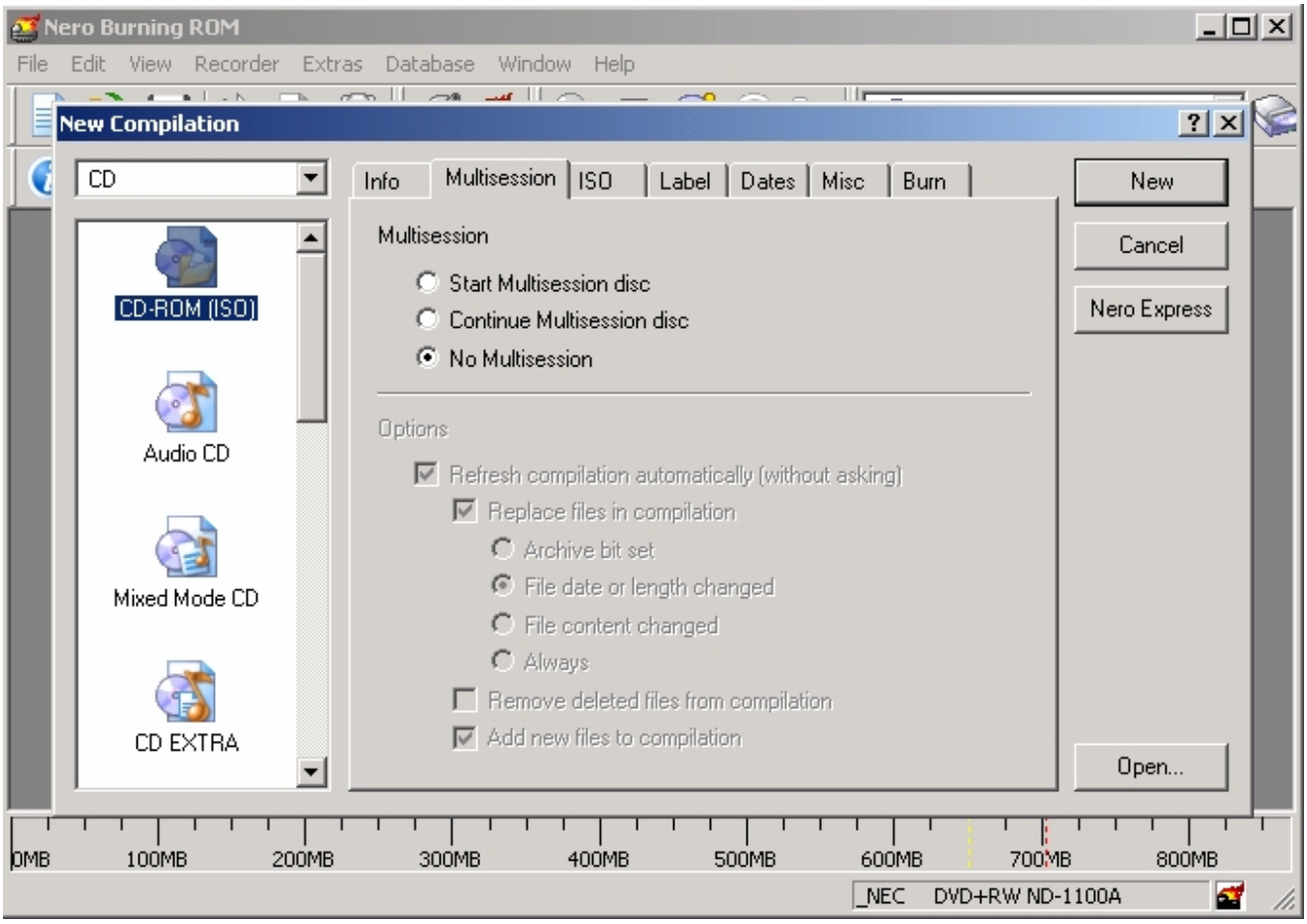
## Brief Information of Naming the File

Software version differs from each other depending on front models, loader type etc. Each character in the file name is an abbreviation of a description as illustrated below.

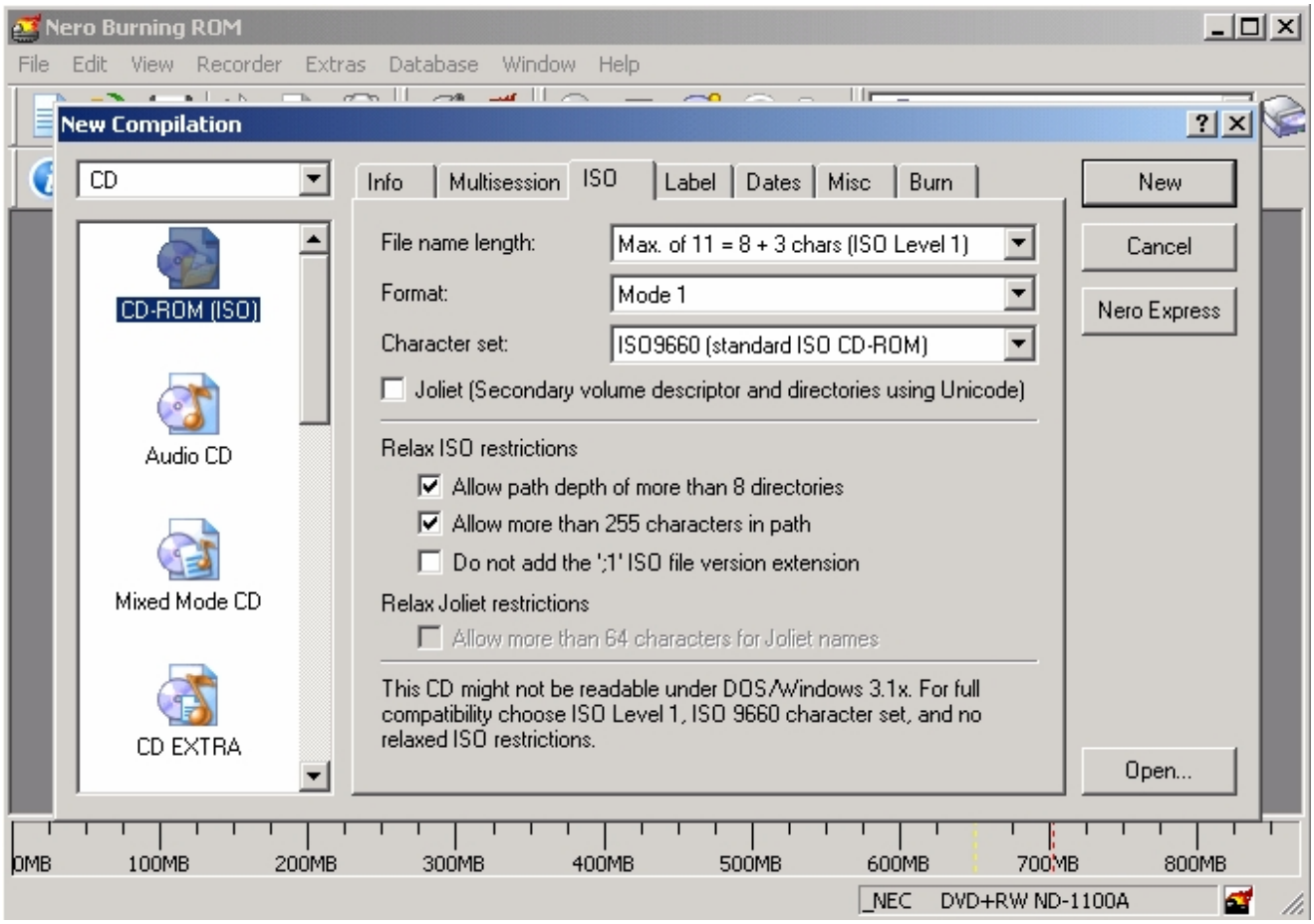




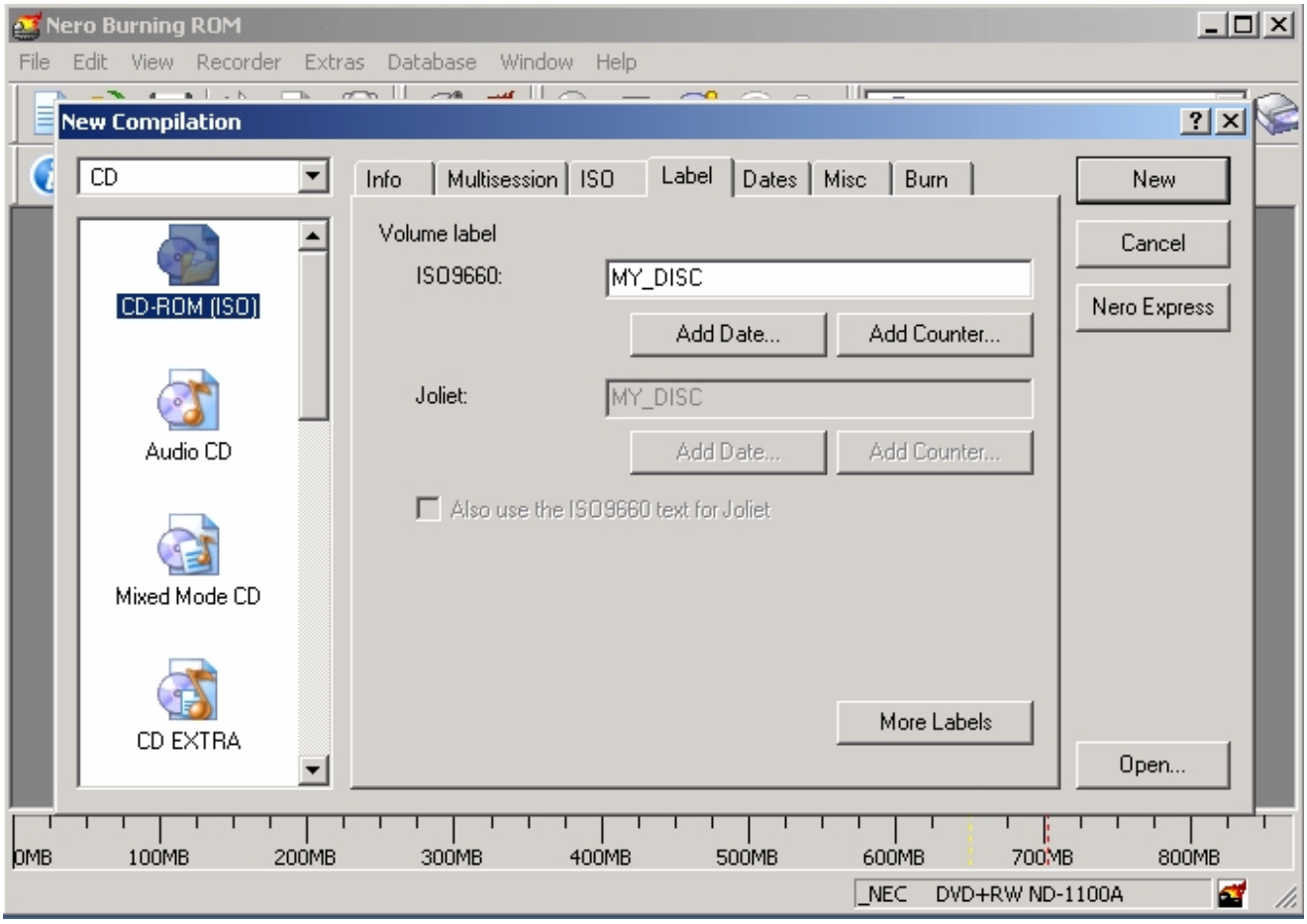

Pay attention the left side. Select **CD and CD_ROM (ISO)** on the upper left side of screen

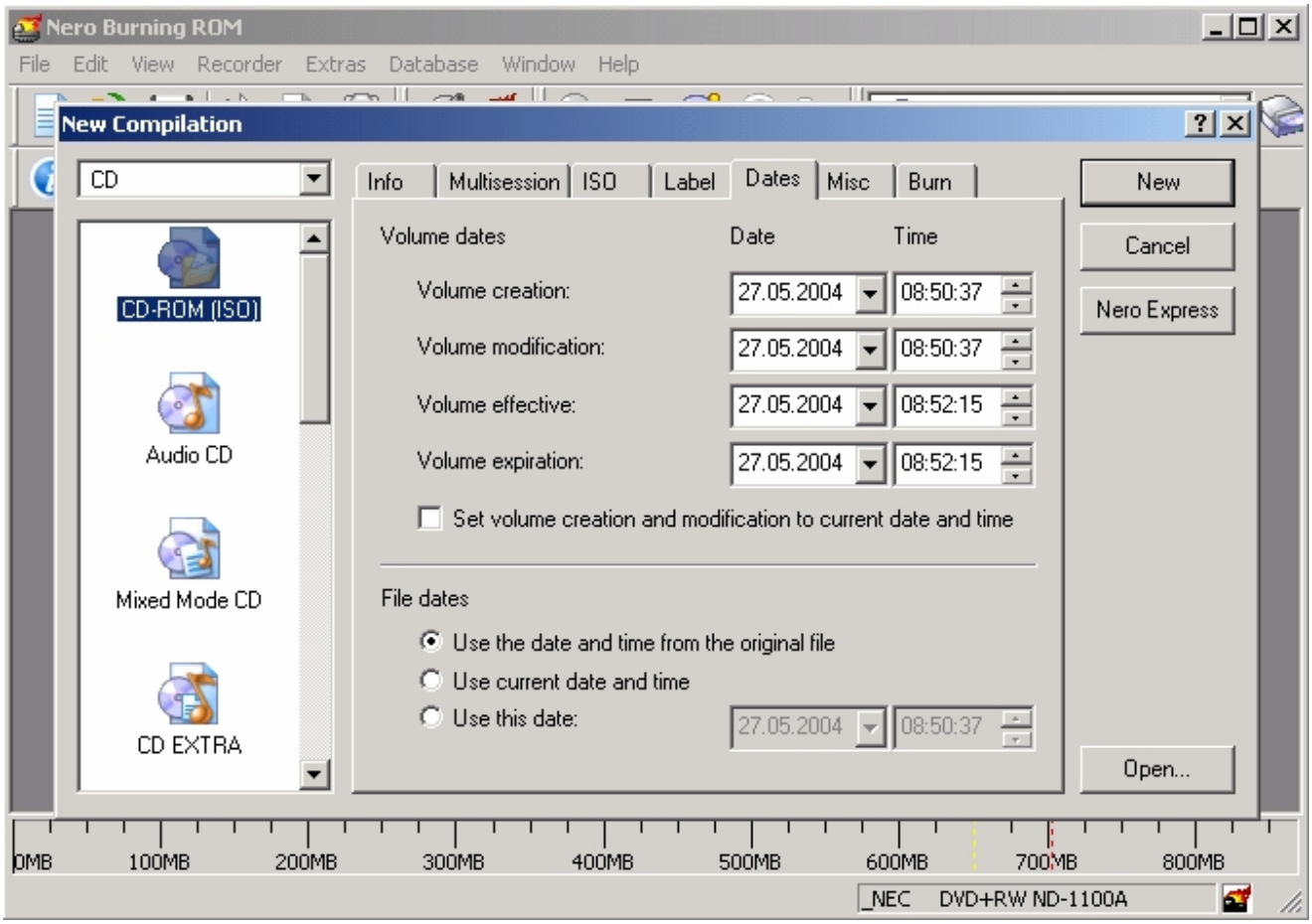



Select **No Multisession**




Format is **Mode 1**


Nero Burning ROM
File Edit View Recorder Extras Database Window Help
New Compilation
CD
CD-ROM (ISO)
Audio CD
Mixed Mode CD
CD EXTRA
Info Multisession ISO Label Dates Misc Burn
Volume label
ISO9660: MY_DISC
Add Date... Add Counter...
Joliet: MY_DISC
Add Date... Add Counter...
Also use the ISO9660 text for Joliet
More Labels
New
Cancel
Nero Express
Open...
0MB 100MB 200MB 300MB 400MB 500MB 600MB 700MB 800MB
_NEC DVD+RW ND-1100A

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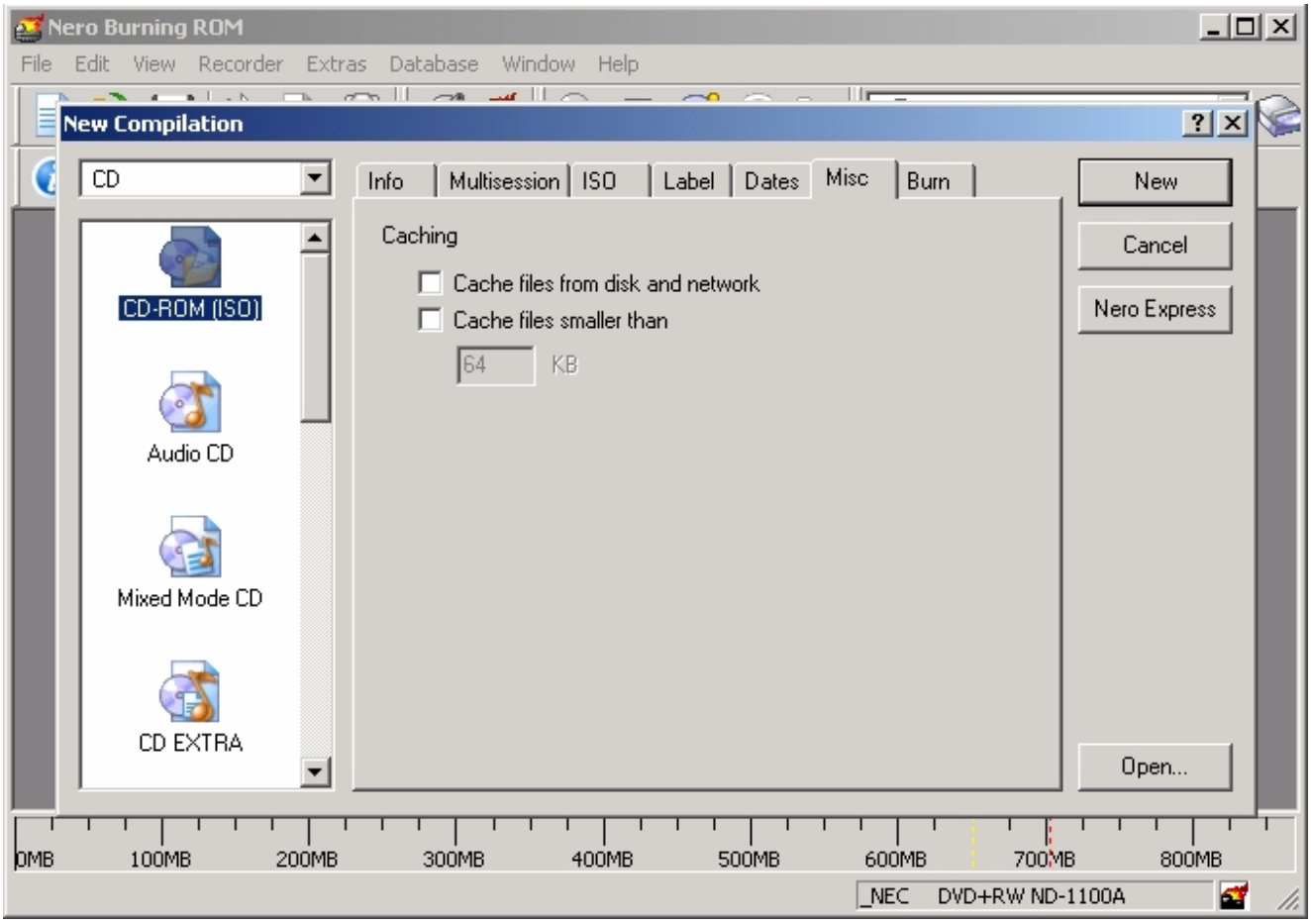


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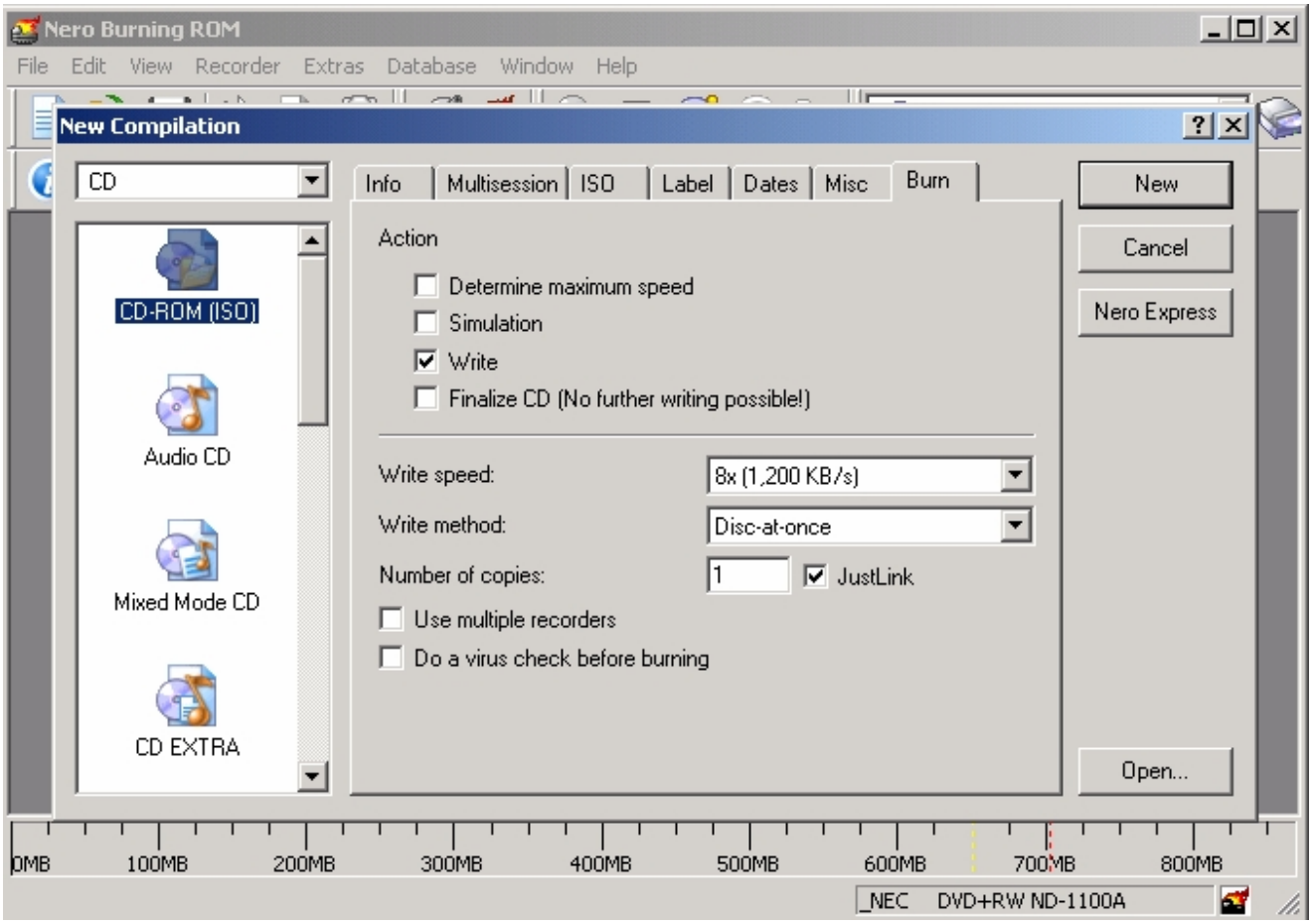
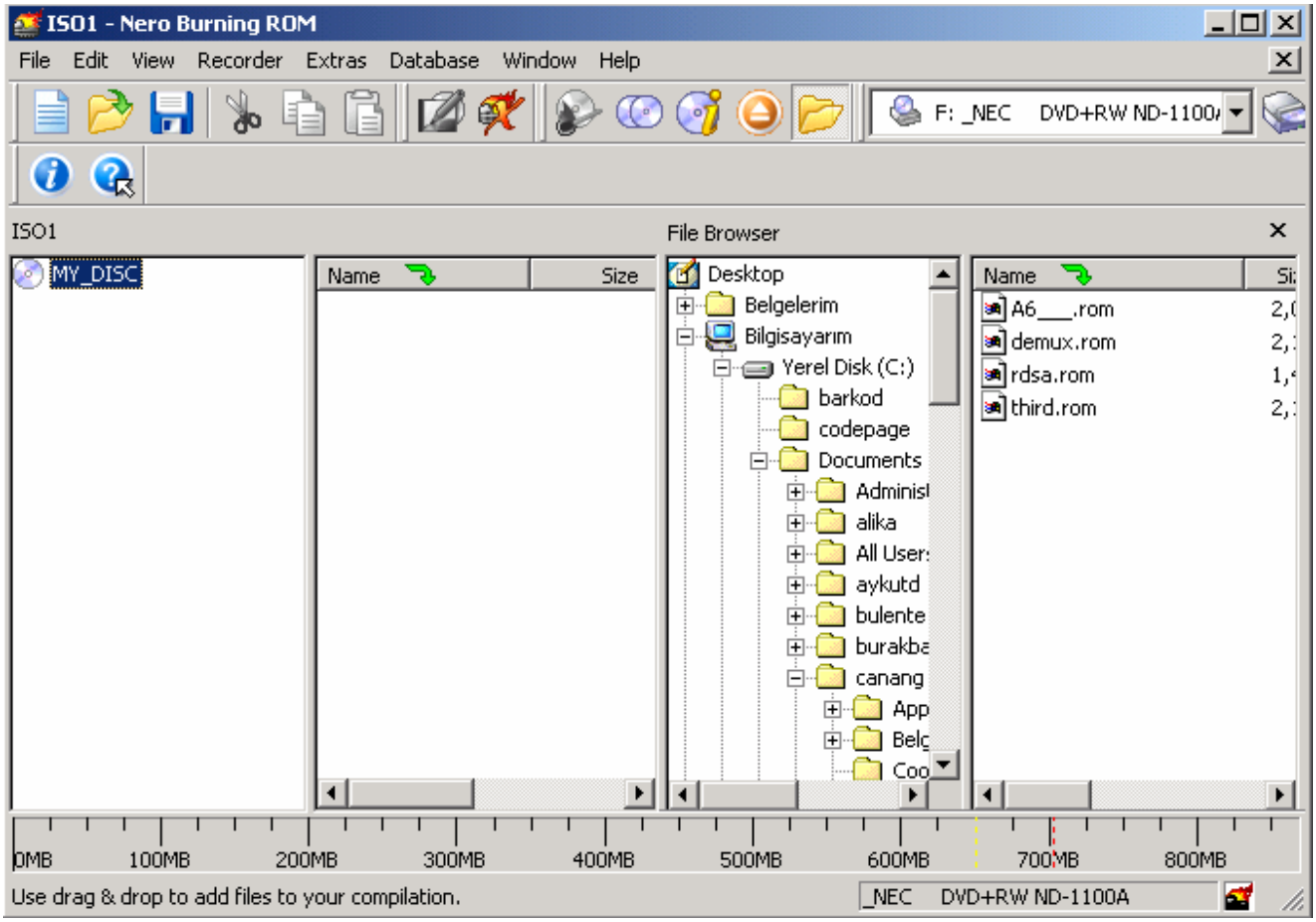
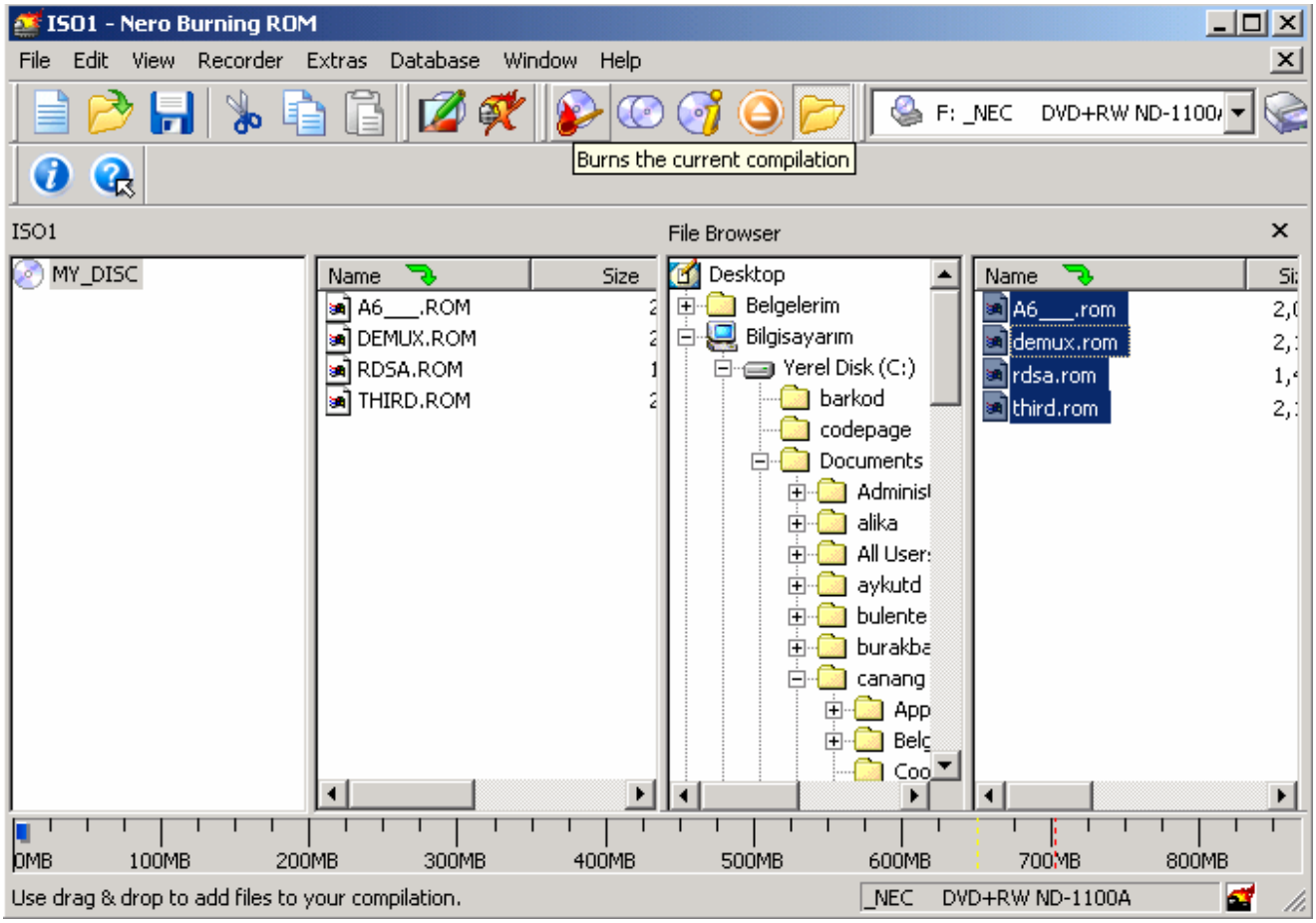


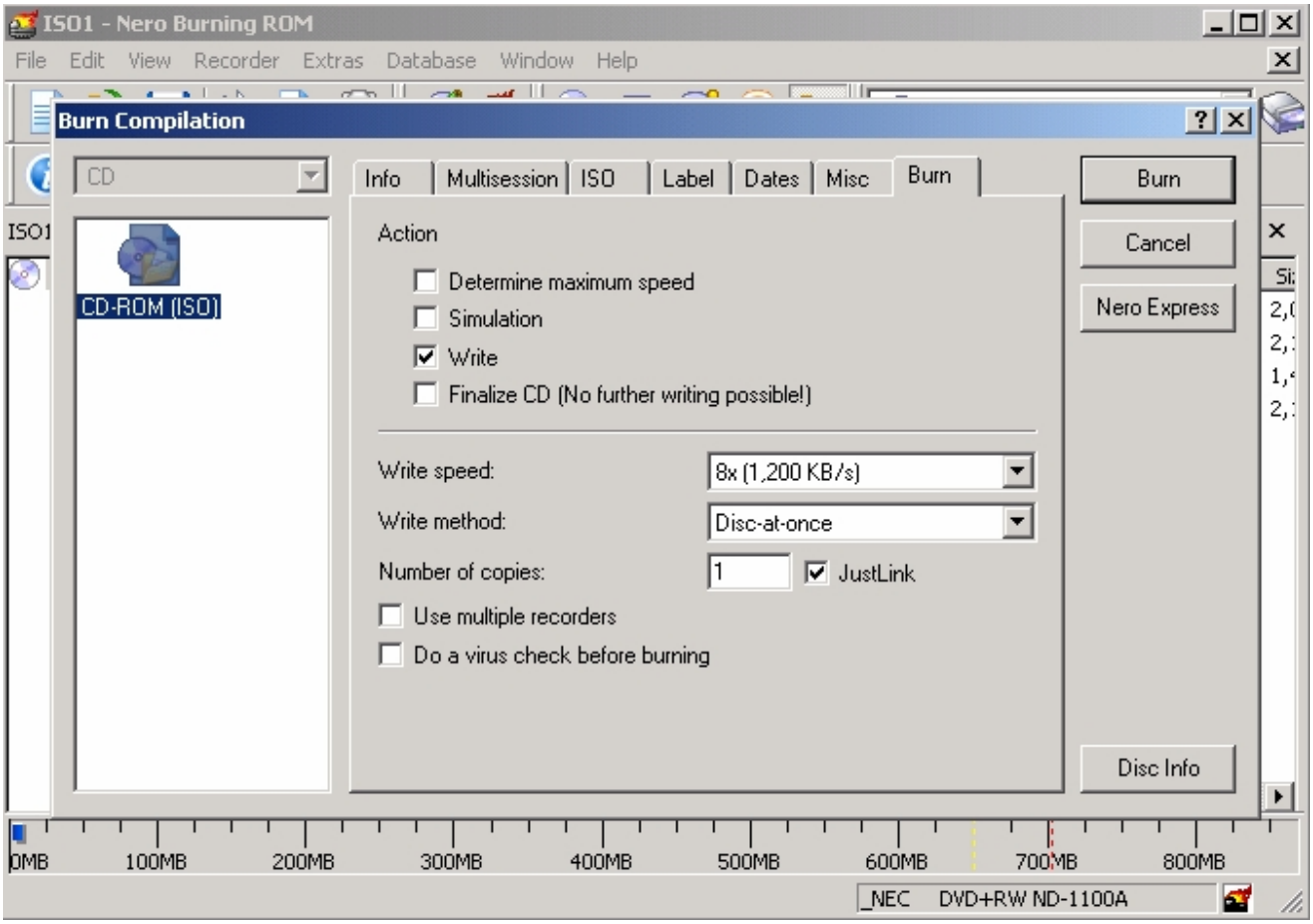

Click the “New” on the upper right corner  of the screen



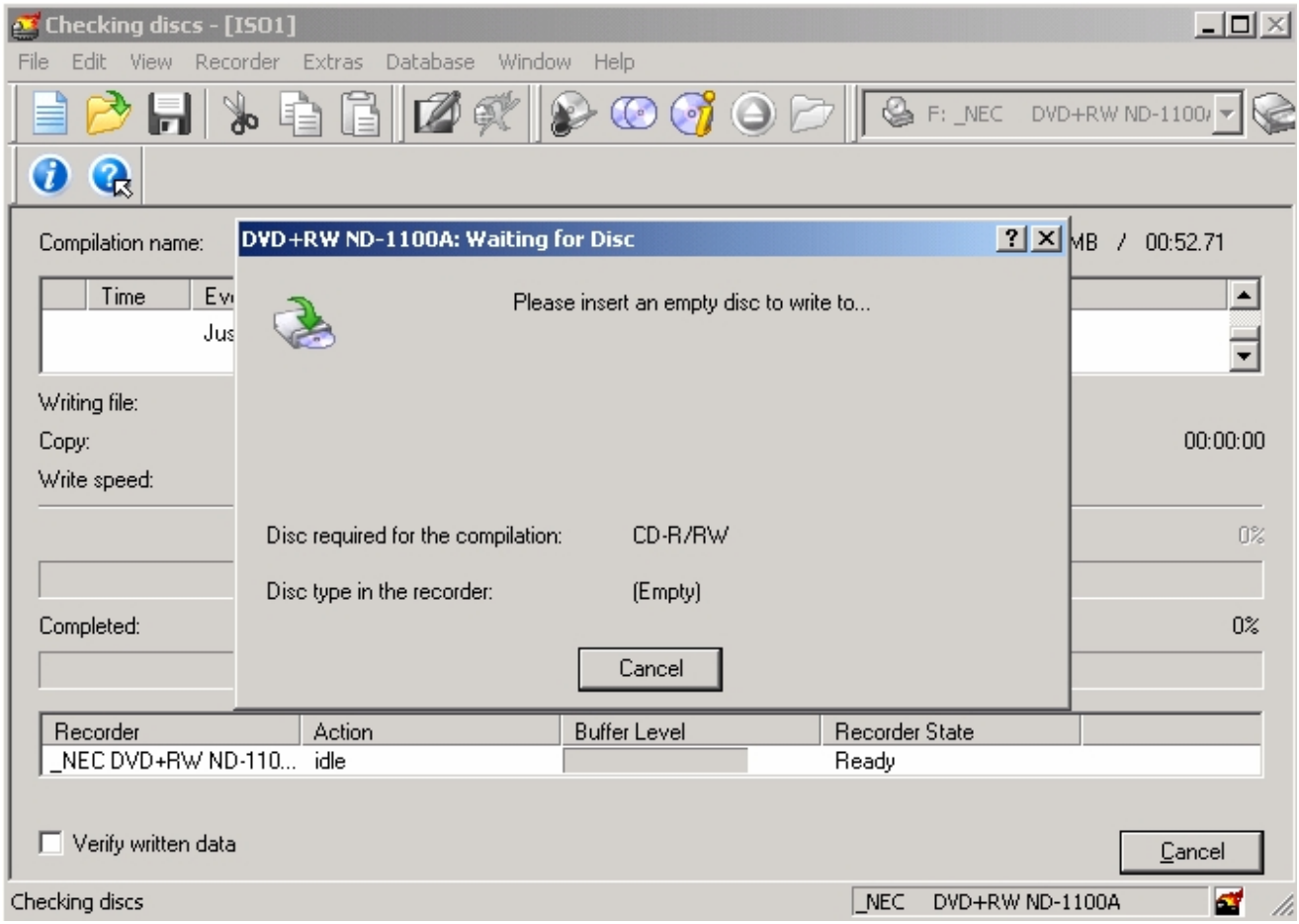

Select your file from file browser then you will see your file in the “Name” section on the right side and then copy the files to under “Name” section on the left side.(this is just an example you will see your file name when you are doing this process)




Click the “Burns the current compilation”




Then you will see this screen and click the “Burn” on the right upper side of screen




You will see this screen and tray will open itself on computer ,then place the CD in CD-ROM
And it will start writing. At the end you will see “burn complited”

# VESTEL-4500 ——— ES68xx + KHM310/DL3CH + OUTPUT

Layout--------VESTEL-4500-A4B4

## Background

This DVD design is based on ESS ES68xx single chip DVD mpeg and servo processor. The ES68xx is buil t upon ESS proven Programmable Multimedia Processor architecture with integrated servo DSP. A comple te DVD design using ES6603 RF-Amp can support all major popular optical pickup heads. With ES68xx unify memory architecture, the whole system memory is reduced to a minimum. ES68xx provides the best pr ice performance DVD solution in the industry and include the latest MPEG4/DivX playback c apability.

andy_ho@esstech.com.hk

## System Clock Requirement

ES68xx require a 27MHz clock to operate. This 27MHz can either b e generated externally and feed into pin 193 and pin 195 or thru a 27MHz crystal attached to pin 193 and 19 4. This 27Mhz will be used for all video processing reference. In addition, internal multiplier will generate a much higher operatin g frequency for the internal RISC+DSP code to operate. Audio clock is generated from ES68xx by its int ernal PLL circuitry.

## SDRAM Usage

ES68xx supports different SDRAM configuration from 1Mx16, 4Mx16 to 8Mx16 S DRAM. The basic requirement can go as low to 2 pcs of 1Mx16 SDRAM with standard feature set. You can also ma ke use of 8Mx16 SDRAM to achieve longer ESP antishock time for portable appl ication.

## System Configuration

| CHIP | FUNCTION |
|---|---|
| ES68xx | Single chip processor that handles all system control , DVD decoding and servo control. |
| 32/64MBit SDRAM | Data storage and frame buffer using either 1 pc of 4Mx16 SDRAM or 2 pcs of 1Mx16 SDRAM |
| 4/8Mbit EPROM/FLASH | Program storage using either 4Mbit Flash o r 8Mbit Flash |
| 24C01 SERIAL EE | System setup configuration storage |

| LCSx# | FUNCTION |
|---|---|
| LCS0# | RAM |
| LCS1# | I/O expand |
| LCS2# | FLASH |
| LCS3# | ROM/FLASH |

| AUXx | FUNCTION |
|---|---|
| AUX0 | I2C DATA |
| AUX1 | I2C CLOCK |
| AUX2 | VFD DATA |
| AUX3 | AUDIO BUFFER CONTROL |
| AUX4 | IR/SPARE |
| AUX5 | AMP_PWR/DFCT |
| AUX6 | VFD CS# |
| AUX7 | VFD CLK/IR |

| AUXxx | FUNCTION |
|---|---|
| 00 | SCARTCTL0 |
| 01 | SCARTCTL1 |
| 02 | ate_en |
| 03 | SCARTCTL2 |
| 12 | RXD1 |
| 13 | TXD1 |
| 14 | RXD0 |
| 15 | TXD0 |
| 16 | HSYNC |
| 17 | VSYNC |
| 30 | SPARE |
| 31 | SPARE |
| 32 | SPARE/VFDCLK |
| 33 | SPARE |
| 34 | SPARE |
| 35 | SPARE |
| 36 | SPARE |
| 37 | SPARE |

### EXPANSION I/O

| XAUXx | FUNCTION |
|---|---|
| 0 | SPARE |
| 1 | SPARE |
| 2 | SPARE |
| 3 | SPARE |
| 4 | SPARE |
| 5 | SPARE |
| 6 | SPARE |
| 7 | SPARE |

## Revision History

Rev-A1
Base on ESS NEO-A8

Rev-A2
1.Delete P9.

2.Change P1 package net.

Rev-A3

1.Change (U2.12),(U7.1),net to RESET#.

Rev-A4

1.Reset IC power for 3 .3V to 5V

2.added Capacities C22 -23,C26-29.

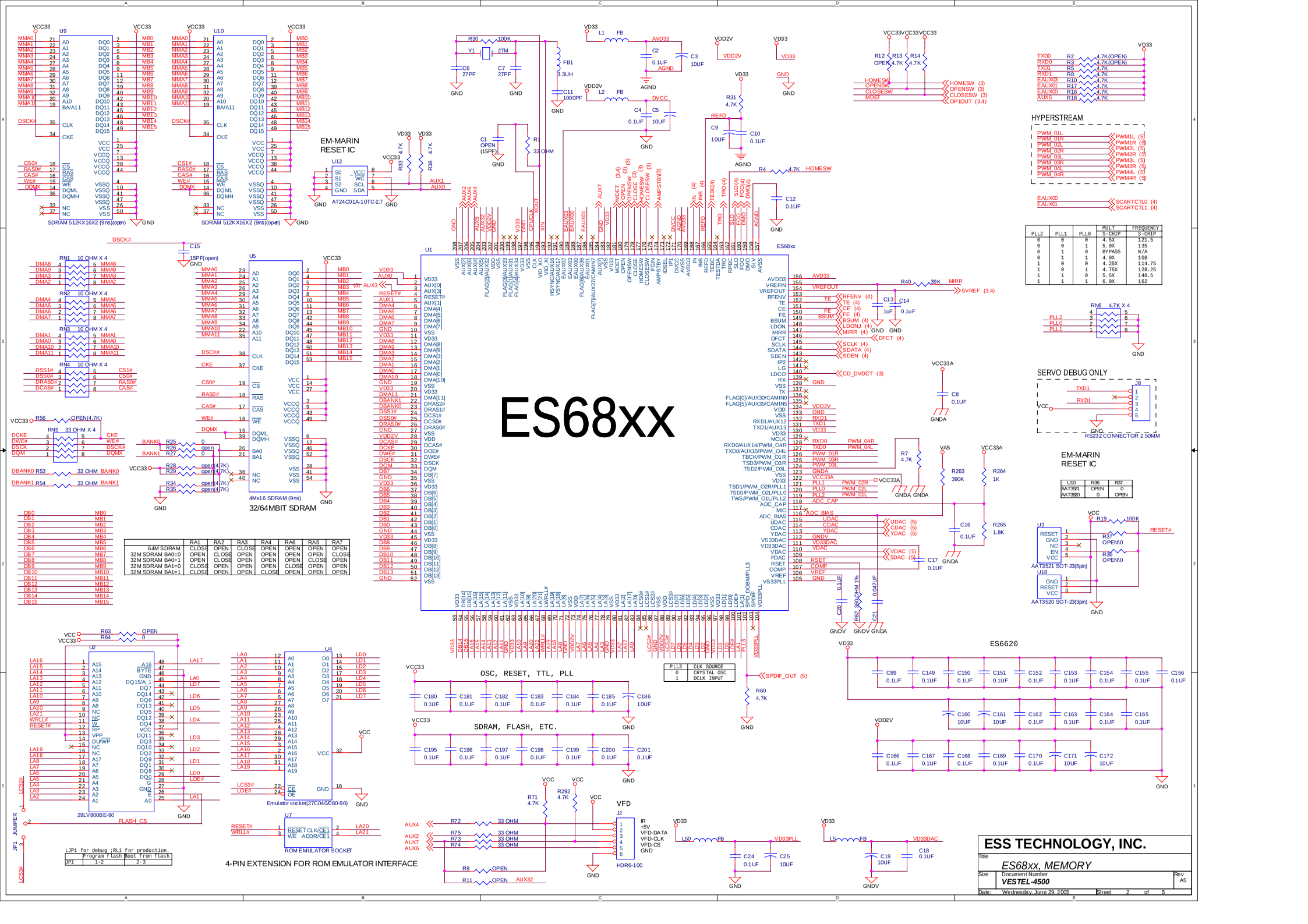
Rev-A5
1.Added Resistor R20,R32.

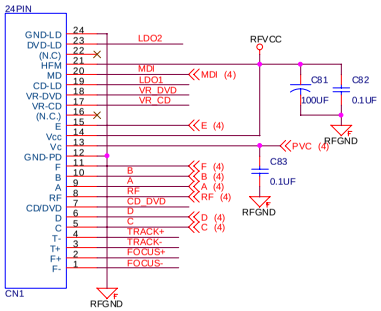
**ESS TECHNOLOGY, INC.**

Title: *INDEX*

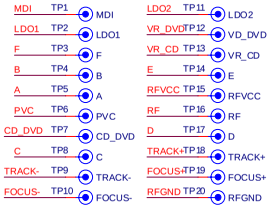
Size | Document Number: ***VESTEL-4500*** | Rev: A5

Date: Wednesday, June 29, 2005 | Sheet 1 of 5

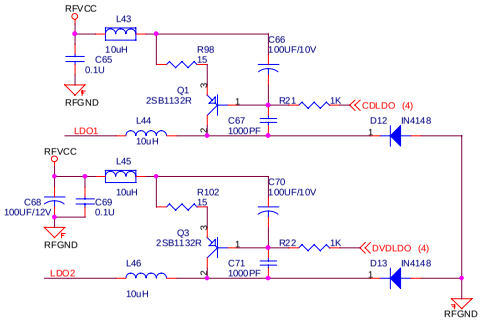

ES68xx
32/64MBIT SDRAM
EM-MARIN RESET IC
OSC, RESET, TTL, PLL
SDRAM, FLASH, ETC.
VFD
ES6620
HYPERSTREAM
SERVO DEBUG ONLY
4-PIN EXTENSION FOR ROM EMULATOR INTERFACE
ROM EMULATOR SOCKET
ESS TECHNOLOGY, INC.
ES68xx, MEMORY
VESTEL-4500

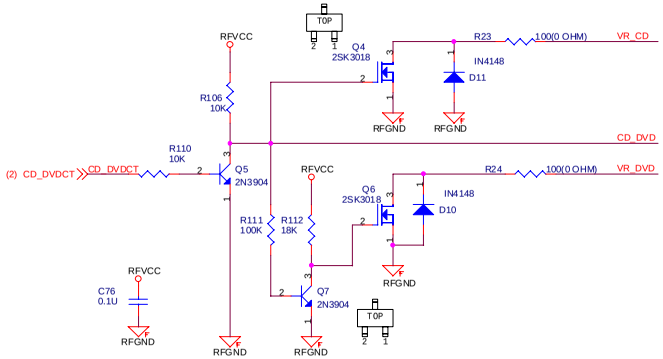


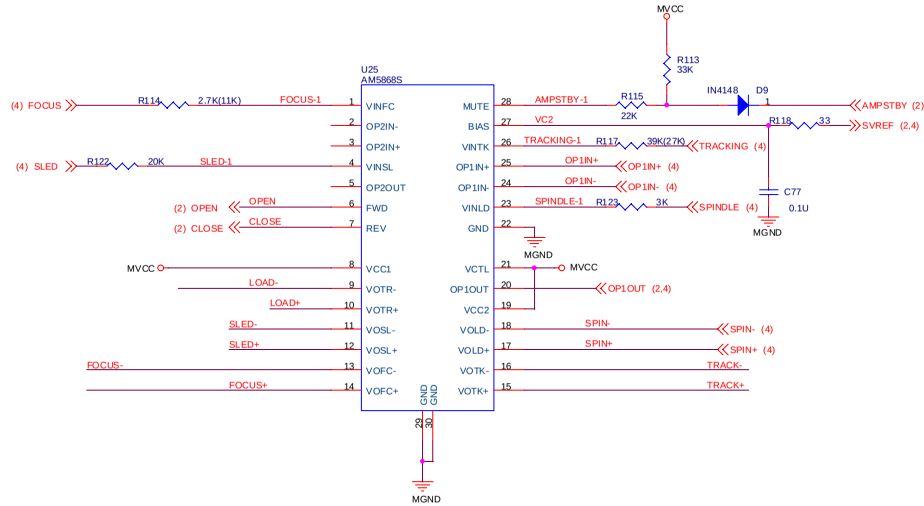

KHM310(IDM510)

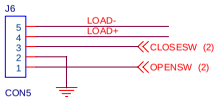


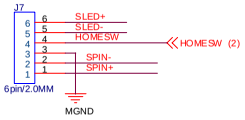

| | KHM310 | DL3CH |
|---|---|---|
| R23 | 100 | 0 |
| R24 | 100 | 0 |
| R114 | 2.7K | 11K |
| R117 | 39K | 27K |

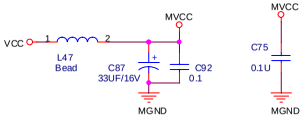


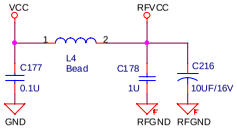



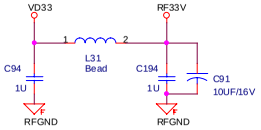

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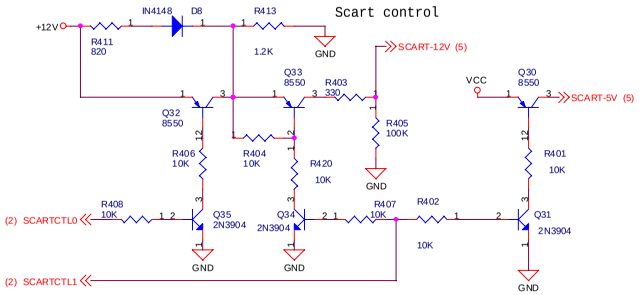
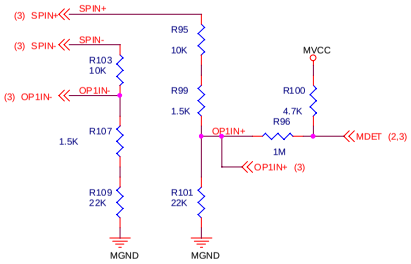
Title: *OPU, MOTOR, POWER*

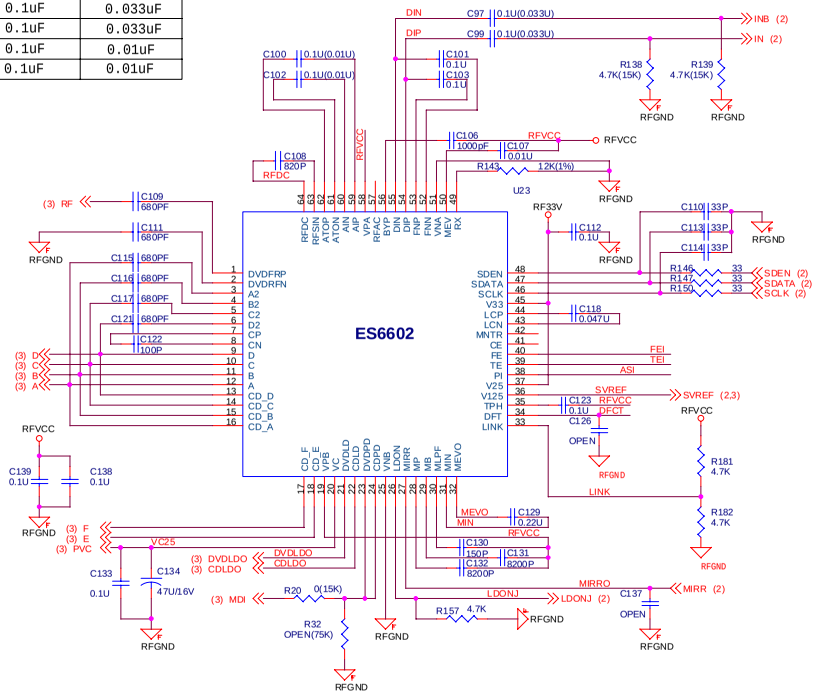
Size | Document Number: ***VESTEL-4500*** | Rev: A5

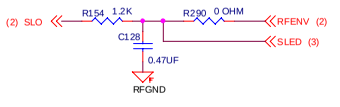
Date: Wednesday, June 29, 2005 | Sheet 3 of 5

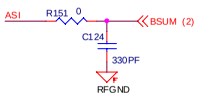
| | KHM310 | DL3CH |
|---|---|---|
| R20 | 0 | 15K |
| R32 | OPEN | 75K |
| C97 | 0.1uF | 0.033uF |
| C99 | 0.1uF | 0.033uF |
| C100 | 0.1uF | 0.01uF |
| C102 | 0.1uF | 0.01uF |

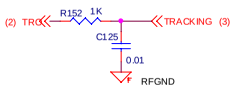


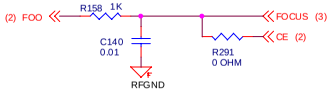



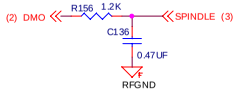



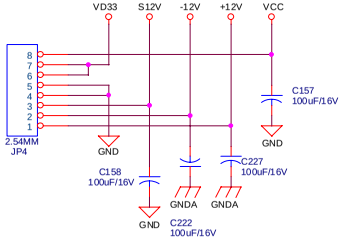



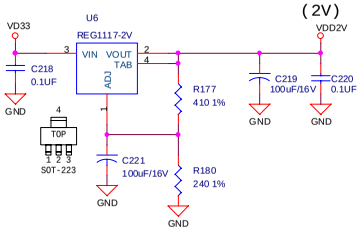



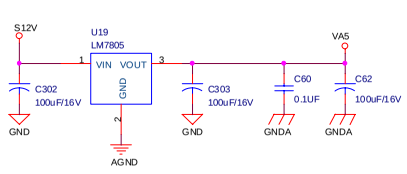



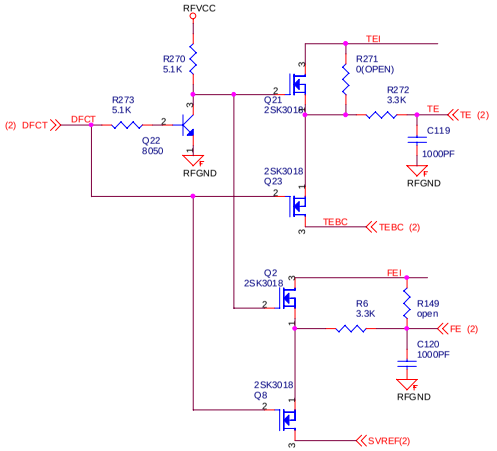



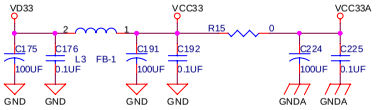



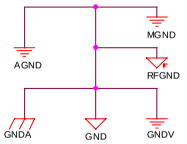




| | | |
|---|---|---|
| ESS TECHNOLOGY, INC. | | |
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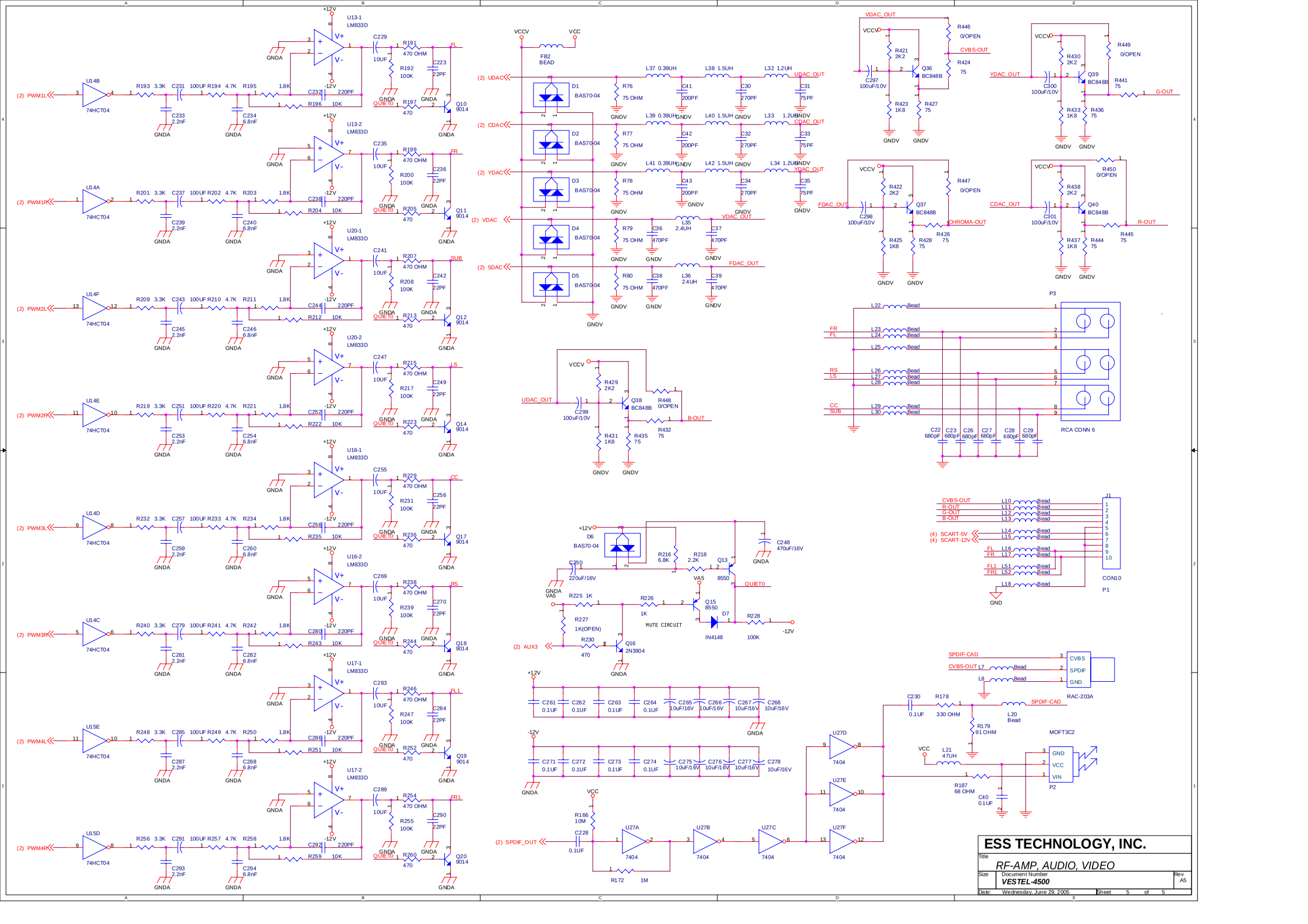
| Size | Document Number: ***VESTEL-4500*** | Rev: A5 |
| Date: Wednesday, June 29, 2005 | Sheet 4 of 5 | |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74HCT04
(2) PWM1L
R193 3.3K
C231 100UF
R194 4.7K
R195 1.8K
C232 220PF
R196 10K
C233 2.2nF
C234 6.8nF
U13-1
LM833D
C229 10UF
R191 470 OHM
R192 100K
C223 22PF
R197 470
Q10 9014
FL
U14.A
(2) PWM1R
R201 3.3K
C237 100UF
R202 4.7K
R203 1.8K
C238 220PF
R204 10K
C239 2.2nF
C240 6.8nF
U13-2
LM833D
C235 10UF
R199 470 OHM
R200 100K
C236 22PF
R205 470
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FR
U14.F
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C243 100UF
R210 4.7K
R211 1.8K
C244 220PF
R212 10K
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C246 6.8nF
U20-1
LM833D
C241 10UF
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R208 100K
C242 22PF
R213 470
Q12 9014
SUB
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C251 100UF
R220 4.7K
R221 1.8K
C252 220PF
R222 10K
C253 2.2nF
C254 6.8nF
U20-2
LM833D
C247 10UF
R215 470 OHM
R217 100K
C249 22PF
R223 470
Q14 9014
LS
U14.D
(2) PWM3L
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C257 100UF
R233 4.7K
R234 1.8K
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R235 10K
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C260 6.8nF
U16-1
LM833D
C255 10UF
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R231 100K
C256 22PF
R236 470
Q17 9014
CC
U14.C
(2) PWM3R
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C279 100UF
R241 4.7K
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R243 10K
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LM833D
C269 10UF
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R239 100K
C270 22PF
R244 470
Q18 9014
RS
U15.E
(2) PWM4L
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R249 4.7K
R250 1.8K
C286 220PF
R251 10K
C287 2.2nF
C288 6.8nF
U17-1
LM833D
C283 10UF
R246 470 OHM
R247 100K
C284 22PF
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Q19 9014
FL1
U15.D
(2) PWM4R
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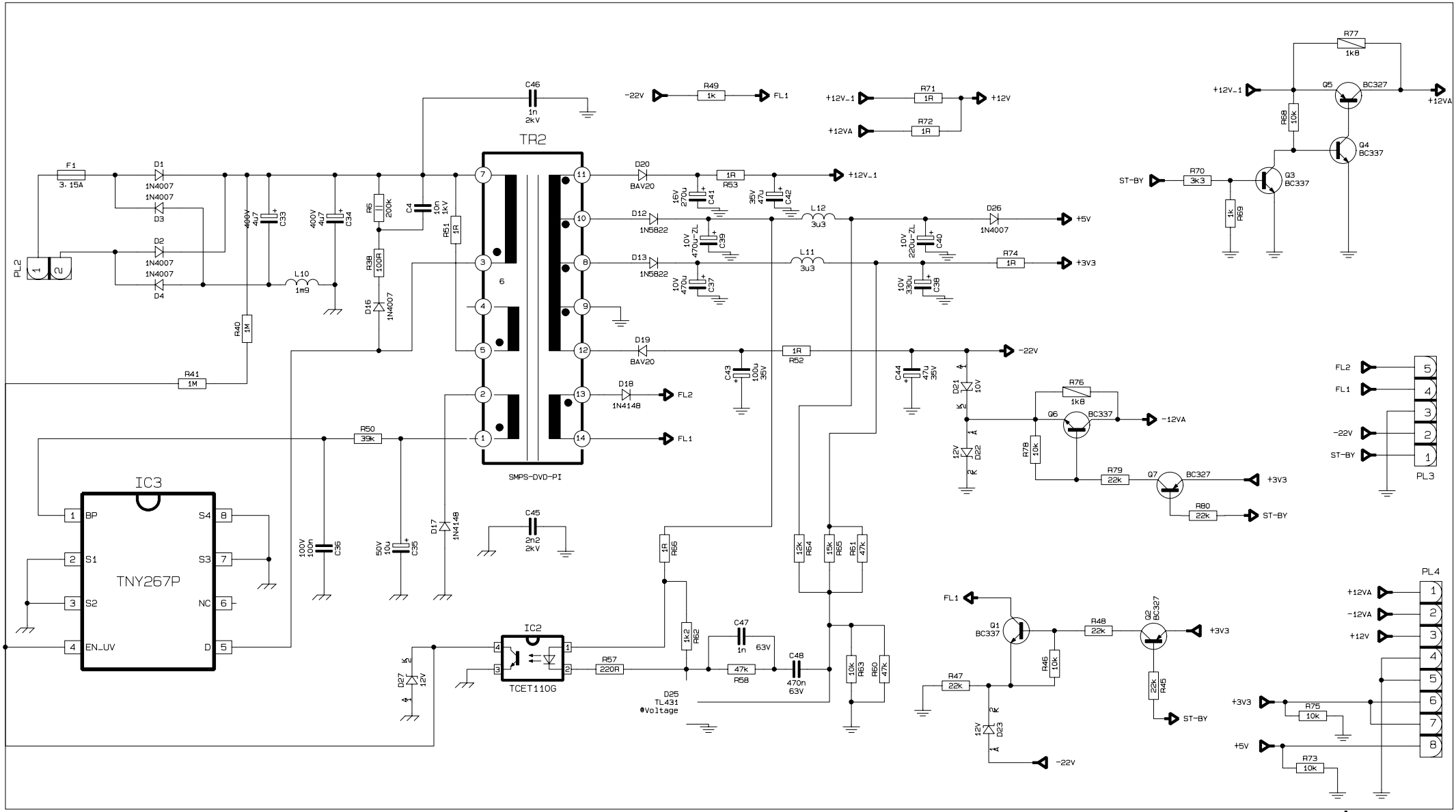
C291 100UF
R257 4.7K
R258 1.8K
C292 220PF
R259 10K
C293 2.2nF
C294 6.8nF
U17-2
LM833D
C289 10UF
R254 470 OHM
R255 100K
C290 22PF
R260 470
Q20 9014
FR1
+12V
-12V
GNDA
QUIET0
74HCT04
(2) UDAC
(2) CDAC
(2) YDAC
(2) VDAC
(2) SDAC
VCCV
VCC
FB2
BEAD
D1 BAS70-04
D2 BAS70-04
D3 BAS70-04
D4 BAS70-04
D5 BAS70-04
L37 0.39UH
L38 1.5UH
L32 1.2UH
L39 0.39UH
L40 1.5UH
L33 1.2UH
L41 0.39UH
L42 1.5UH
L34 1.2UH
L35 2.4UH
L36 2.4UH
R76 75 OHM
R77 75 OHM
R78 75 OHM
R79 75 OHM
R80 75 OHM
C41 200PF
C42 200PF
C43 200PF
C36 470PF
C38 470PF
C30 270PF
C32 270PF
C34 270PF
C37 470PF
C39 470PF
C31 75PF
C33 75PF
C35 75PF
UDAC_OUT
CDAC_OUT
YDAC_OUT
VDAC_OUT
FDAC_OUT
GNDV
VDAC_OUT
R446 0/OPEN
CVBS-OUT
R424 75
R421 2K2
Q36 BC848B
C297 100uF/10V
R423 1K8
R427 75
YDAC_OUT
R449 0/OPEN
R430 2K2
Q39 BC848B
C300 100uF/10V
R433 1K8
R436 75
R441 75
G-OUT
FDAC_OUT
R447 0/OPEN
R422 2K2
Q37 BC848B
C298 100uF/10V
R425 1K8
R428 75
CHROMA-OUT
R426 75
CDAC_OUT
R450 0/OPEN
R438 2K2
Q40 BC848B
C301 100uF/10V
R437 1K8
R444 75
R-OUT
R445 75
P3
L22 Bead
L23 Bead
L24 Bead
L25 Bead
L26 Bead
L27 Bead
L28 Bead
L29 Bead
L30 Bead
FR
FL
RS
LS
CC
SUB
C22 680pF
C23 680pF
C26 680pF
C27 680pF
C28 680pF
C29 680pF
RCA CONN 6
UDAC_OUT
R429 2K2
Q38 BC848B
C299 100uF/10V
R448 0/OPEN
B-OUT
R431 1K8
R435 75
R432 75
D6 BAS70-04
C250 220uF/16V
R216 6.8K
R218 2.2K
Q13 8550
C248 470uF/16V
VA5
R225 1K
R226 1K
Q15 8550
QUIET0
R227 1K(OPEN)
MUTE CIRCUIT
D7 IN4148
R228 100K
(2) AUX3
R230 470
Q16 2N3904
CVBS-OUT
R-OUT
G-OUT
B-OUT
(4) SCART-5V
(4) SCART-12V
FL
FR
FL1
FR1
L10 Bead
L11 Bead
L12 Bead
L13 Bead
L14 Bead
L15 Bead
L16 Bead
L17 Bead
L51 Bead
L52 Bead
L18 Bead
GND
J1
CON10
P1
C261 0.1UF
C262 0.1UF
C263 0.1UF
C264 0.1UF
C265 10uF/16V
C266 10uF/16V
C267 10uF/16V
C268 10uF/16V
C271 0.1UF
C272 0.1UF
C273 0.1UF
C274 0.1UF
C275 10uF/16V
C276 10uF/16V
C277 10uF/16V
C278 10uF/16V
(2) SPDIF_OUT
R166 10M
C228 0.1UF
R172 1M
U27A
U27B
U27C
U27D
U27E
U27F
7404
SPDIF-CAD
CVBS-OUT
L7 Bead
L8 Bead
CVBS
SPDIF
GND
RAC-203A
C230 0.1UF
R178 330 OHM
L20 Bead
R179 91 OHM
L21 47UH
R187 68 OHM
C40 0.1UF
MOFT3C2
VIN
P2
ESS TECHNOLOGY, INC.
Title
RF-AMP, AUDIO, VIDEO
Size
Document Number
VESTEL-4500
Rev
A5
Date: Wednesday, June 29, 2005
Sheet 5 of 5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IC2
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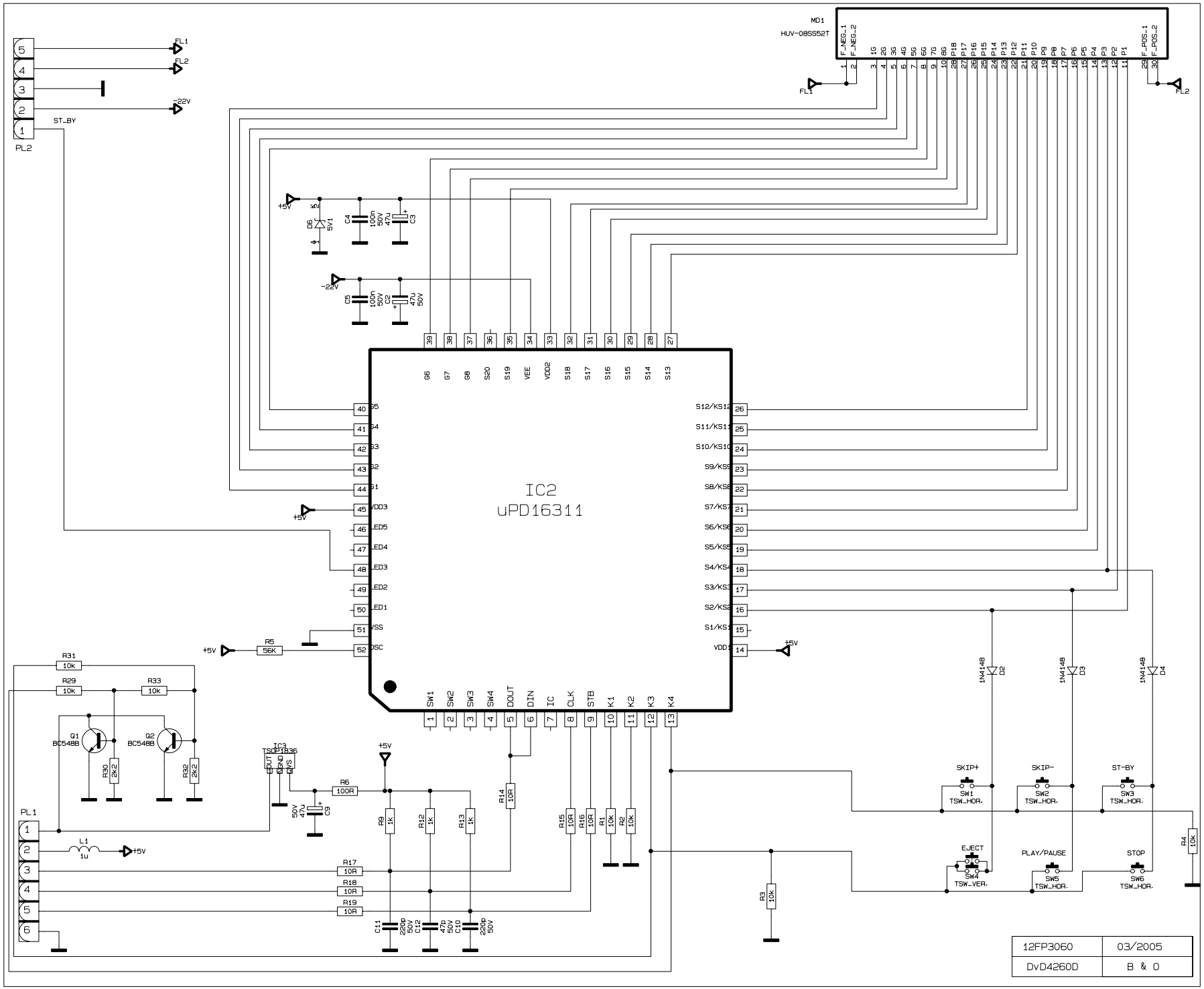
D25
TL431
@Voltage
PL2
PL3
PL4
F1
3. 15A
L10
1mg
L11
3u3
L12
3u3
-22V
+12V_1
+12V
+12VA
+5V
+3V3
-12VA
ST-BY
FL1
FL2


MD1
HUV-08SS52T
F_NEG-1
F_NEG-2
F_POS-1
F_POS-2
FL1
FL2
PL2
ST_BY
-22V
+5V
IC2
uPD16311
D6
5V1
C4
100n
50V
C3
47u
C5
C2
R5
56K
R31
10k
R29
R33
Q1
BC548B
Q2
R30
2k2
R32
IC3
TSD1835
R6
100R
C9
PL1
L1
1u
R9
1k
R12
R13
R14
10R
R15
R16
R1
R2
R17
R18
R19
C11
220p
C12
C10
R3
1N4148
D2
D3
D4
SKIP+
SKIP-
ST-BY
SW1
SW2
SW3
TSW_HOR.
EJECT
PLAY/PAUSE
STOP
SW4
SW5
SW6
TSW_VER.
R4
12FP3060
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DvD4260D
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